Space Programs Summary No. 37-27, Volume III

for the period March 1, 1964 to April 30, 1964

The Deep Space Network

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JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
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Preface

The *Space Programs Summary* is a six volume, bimonthly publication designed to report on JPL space exploration programs, and related supporting research and advanced development projects. The subtitles of all volumes of the *Space Programs Summary* are:

Vol. I. The Lunar Program (Confidential)

Vol. II. The Planetary–Interplanetary Program (Confidential)

Vol. III. The Deep Space Network (Unclassified)

Vol. IV. Supporting Research and Advanced Development (Unclassified)

Vol. V. Supporting Research and Advanced Development (Confidential)

Vol. VI. Space Exploration Programs and Space Sciences (Unclassified)

The *Space Programs Summary,* Volume VI consists of an unclassified digest of appropriate material from Volumes I, II, and III and a reprint of the space science instrumentation studies of Volumes I and II.

Beginning with the *Space Programs Summary 37-27* series, the Space Flight Operations Facility development progress, previously reported in Volume VI, will be reported in Volume III. The scope of Volume III is being expanded to incorporate the activities of the Deep Space Network.

W. H. Pickering, *Director*
Jet Propulsion Laboratory

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Contents

I. Introduction

The Deep Space Network (DSN) is a precision communication system which is designed to communicate with, and permit control of, spacecraft designed for deep space exploration. The DSN consists of the Deep Space Instrumentation Facility (DSIF), the Space Flight Operations Facility (SFOF), and the DSN Ground Communication System (GCS).

The DSIF utilizes large antennas, low-noise phase-lock receiving systems and high-power transmitters located at stations positioned approximately 120 deg around the Earth to track, command and receive data from deep space probes. Overseas stations are generally operated by personnel of the respective countries. The DSIF stations are:

I.D. No.	Name	Location
11	Goldstone, Pioneer	Goldstone, California
12	Goldstone, Echo	Goldstone, California
13	Goldstone, Venus (R&D)	Goldstone, California
14	Goldstone, Mars (under construction)	Goldstone, California
41	Woomera	Island Lagoon, Australia
42	Canberra (under construction)	Canberra, Australia
51	Johannesburg	Johannesburg, South Africa
61	Madrid (under construction)	Madrid, Spain
71	Spacecraft Monitoring	Cape Kennedy, Florida

The SFOF is located in a three-story building at the Jet Propulsion Laboratory in Pasadena, California, and utilizes operations control consoles, status and operations displays, computers, data processing equipment for analysis of spacecraft performance and space science experiments, and communication facilities to control space flight operations. This control is accomplished by generating trajectories and orbits, and command and control data, from tracking and telemetry data received from the DSIF in near real time. The SFOF also reduces the telemetry, tracking, command and station performance data recorded by the DSIF into engineering and scientific information for analysis and use by the scientific experimenters and spacecraft engineers.

The DSN Ground Communication System consists of: voice, normal and high data rate teletype circuits provided by the NASA World-Wide Communications Network between each overseas station and the SFOF; and teletype and voice circuits between the SFOF, Goldstone stations and Cape Kennedy, and a microwave link between the SFOF and Goldstone, provided by the DSN.

The DSN has facilities for simultaneously controlling a newly launched spacecraft and a second one already in flight and, within a few months, will be able to control simultaneously either two newly launched spacecraft plus two in flight, or the operations of four spacecraft in flight at the same time. The DSIF is equipped with 85-ft antennas having gains of 53 db at 2300 Mc and a system temperature of 55°K, making it possible to receive significant data rates at distances as far as the planet Mars. To improve the data rate and distance capability, a 210-ft antenna is under construction at the Goldstone Mars Station and two additional antennas of this size are scheduled for installation at overseas stations.

It is the policy of the DSN to continuously conduct research and development of new components and systems and to engineer them into the DSN to maintain a state-of-the-art capability.

The DSN is a NASA facility, managed by JPL through a contract between NASA and the California Institute of Technology. The Office of Tracking and Data Acquisition is the cognizant NASA office.

II. Tracking Stations Engineering and Operations

A. Project Engineering

1. Surveyor

A revised version of the *Surveyor* command and data console (CDC) and DSIF interface document has now been published.

The CDC destined for installation at the Goldstone Pioneer Station has been inspected, all its supporting documentation has been reviewed, and it has been shipped to the site where it is being prepared for compatibility tests with the DSIF.

A detailed plan for these tests is being prepared with two major objectives: to verify the CDC–DSIF interface, and to establish the adequacy of the CDC design to perform its intended role in support of *Surveyor*.

2. Pioneer

Copies of the DSIF/Pioneer Program interface document in rough draft form were sent, at the request of Ames Research Center (ARC), to Space Technology Laboratories and to ARC to assist in preparation of the DSN/Pioneer interface document.

The location of Pioneer Program/DSIF interface equipment is under review to resolve the operational problems associated with locating command and telemetering interface equipment remotely from the DSIF control room.

The DSIF digital instrumentation subsystem 910 computer will be used to decommutate the Pioneer Program telemetry data. ARC will furnish necessary 910 computer input–output buffer equipment.

3. Ranger Block III

A memorandum which reviews and evaluates various aspects of the DSIF ground telecommunications RF performance during the *Ranger 6* flight will be published in the *Ranger 6* Operations Analysis Report (OAR). As a special test during the *Ranger 6* flight, the DSIF stations were directed to record received carrier power level during the period of equal range to the spacecraft. The results of this experiment indicated, after correction and weighting procedures, that in 14 station pair comparisons the average disagreement in received carrier power measurements was 1.7 db, collective over all the observations. The maximum disagreement was approximately 4 db; however, most of this discrepancy resulted from a nonstandard RF configuration. The minimum was 0.0 db.

A list of updated DSIF system parameters which are based on actual measurement of antenna gains, system temperatures, and other critical areas has been published. Radiometric measurements of the Echo Station antenna gain have been completed which now allows a transfer of this gain calibration during common spacecraft view to other stations in the net. Phase I of the calibration effort has been completed and Phase II is under way (Ref. 1).

4. Mariner C

Telecommunications compatibility tests of the *Mariner C* spacecraft–DSIF system will be conducted in mid-May 1964. Performance evaluations of both the command system and the telemetry system will be conducted.

An interim spacecraft test facility at the Goldstone antenna range will house the spacecraft equipment. RF signals will be relayed over an approximate 260-db loss link to the Pioneer Station.

The 100-kw Venus site is being prepared for backup support of the *Mariner C* spacecraft. It will be utilized where necessary to interrogate the spacecraft (through the omni-antenna) during the last 3 mo of flight. It will be available on an on-call basis approximately 6 hr after notification. Initial tests of the complete Venus 100-kw site with the *Mariner C* spacecraft are scheduled for February 1965, approximately 3 mo after launch.

B. System Analysis

1. Antenna Gain

In February tests were conducted on the Echo Station antenna, in conjunction with the Communications Element Research Section, in order to obtain a more accurate value for antenna gain. The tests are an attempt to reduce discrepancies in concurrent signal strength measurements from different stations as have been reported during the early *Ranger* and the *Mariner 2* missions. It was felt that by reducing uncertainties in system parameters the stations could be brought closer together in signal levels reported. (See previous discussion, *Ranger Block III*.)

Radiometric measurements of the gain of the Venus site 85-ft Az–El antenna in a Cassegrain configuration have been reported previously (Ref. 2). These measurements were performed at S-band. The approach used on *Echo* was to measure the antenna temperature at L-band, while looking at sources that were used for the Az–El antenna, and relate it to the value obtained with the Az–El, thus obtaining a relative gain figure.

The receiver temperature was calibrated using four different loads which had been built by the Maury Microwave Co. Two of these were nitrogen cooled; the other two were cooled by a mixture of dry ice and acetone. Receiver temperature calibration was accomplished by use of the *Y*-factor method of terminating the receiver input in loads of different temperatures and measuring the difference in power out of the receiver.

The formula relating the ratio of power is

$$Y = \frac{T_r + T_h}{T_r + T_c},$$

where Y is the power ratio, T_r is the receiver temperature, T_h is the temperature of the hot termination and T_c is the temperature of the cold termination. The line connecting the maser input to the diplexer was broken at the diplexer and the loads connected there. Values of Y were obtained between the nitrogen and acetone dry ice loads. In addition, the acetone dry ice load was later replaced by ice water and the *Y*-factor obtained between liquid nitrogen and ice water. Since there is another way to obtain a T_h, one involving use of the noise tube, the noise tube was fired several times for each load, and a *Y*-factor between tube *on* and *off* was obtained. This also permitted determination of the effective temperature of the noise tube.

Combination of *Y*-factor measurements and the number of times each were taken is:

T_c T_h	Number of trials
N_2–CO_2	5
CO_2–H_2O	18
N_2–H_2O	15
N_2–NT	70
NT–CO_2	20
NT–H_2O	24

The result of this procedure, using the method having the smallest error, determined a receiver temperature of $35 \pm 4°K$. The gas tube temperature is approximately $98 \pm 3°K$.

Measurement of star temperatures, taken on M87 and Crab, resulted in data which, when compared with Venus Az–El data, allowed a gain figure to be obtained. The temperature of M87, with the Echo antenna, was measured to be $28 \pm 8°K$, and that of Crab Nebula was $98 \pm 9°K$. The error in measurement was calculated to be $5.2°K + (0.0286)$ (T source). Using the Crab Nebula measurements, the relative gain uncertainty is 0.46 db. Comparison with the Venus Az–El data results in an absolute antenna gain of 45.7 ± 1 db for the Echo L-band horn antenna.

The overseas sites are undergoing modification and new data will have to be obtained for them before a more accurate set of gain and sensitivity figures can be tabulated for the net.

C. System Integration and Engineering

1. Radio Frequency Interference (RFI)

Further measurements of radio frequency interference from fluorescent lights have been planned and suitable lighting fixtures and equipment are being procured for these tests. The measurements will be made as time permits.

2. Spacecraft Test Facility

The plan for implementation of a general purpose spacecraft test facility at Goldstone, described in Ref. 3, has been revised and expanded.

To increase the natural radio path loss between the Goldstone antenna range and the Pioneer Station, it is now intended to house the spacecraft in a radio opaque enclosure 20 ft square and 16 ft high. The spacecraft will be connected to an external radiator via a coaxial line and attenuator. It is contemplated that lunar or planetary path losses of 220 or 270 db, respectively, may be simulated accurately.

The project has financial approval and the facility is scheduled to be available in a simplified form for *Mariner C* tests by the end of May 1964.

3. Station Control and Monitor Console (SCAM)

This project was transferred to the Systems Engineering Group in late January. After receiving information from station managers and reviewing L-band design specification, a new redesign for the S-band system was initiated. A new Phase I prototype specification was written and forwarded to the contractor (Hughes Aircraft Co.) for rebid. Empty console racks, purchased by Hughes under the L-band SCAM contract, were shipped to Goldstone for installation in the S-band control room in order to determine layout requirements. The S-band SCAM (Phase I) will be primarily a system and subsystem status monitor. Phase II (design will begin in May) will utilize the DIS 920 computer for data and station status comparison and assessment and it is planned to display results on a line printer.

4. AMR Spacecraft Monitoring Station, DSIF-71

A draft of a systems study and Project Implementation Document has been prepared and is now being reviewed.

A site acceptable to JPL and NASA has been agreed upon and work is under way at Cape Kennedy on the facilities design.

5. Revision of Technical Memorandum 33-26

The Phase I effort on the revision of *TM 33-26*, which includes an implementation plan, a detailed outline for the new manual, and sections on the RF and Antenna Microwave Subsystems has been submitted by Volt Corp. to JPL for review of content and level of writing. Since it is envisioned that *TM 33-26* will constitute one of the top documents in the DSN documentation tree, it is being prepared with intent to provide sufficient technical system description of the DSIF so that it will be of significant value to agencies contemplating use of the DSIF. It also will be updated periodically.

6. Suitcase Telemetry System

A project implementation plan was prepared for the Suitcase Telemetry System which is designed to supply telemetry coverage for *Mariner C*-type spacecraft at downrange locations where no coverage is presently available. The system will be light enough to be carried as luggage by a two-man team. Critical spacecraft events, such as separation, will be monitored. The present effort

is to determine the feasibility and effectiveness of such a station by attempting to acquire and track the *Mariner C* spacecraft.

Initial studies have shown that for proper coverage two such stations should be employed, one at Johannesburg and one on Mauritius Island. Each station will consist of an antenna and mount, a receiver, a tape recorder, a timing receiver, and associated power supplies.

Initial aircraft tracking tests at Goldstone have indicated that a small 2- to 3-ft circular polarized antenna, mounted on a tripod with an azimuth–elevation mount will probably be satisfactory. A wide beamwidth antenna (15 to 20 deg) is required to facilitate acquisition. The receiver will be a modification of the *Mariner C* spacecraft transponder receiver and will employ an IF bandwidth of 4.5 kc, a threshold loop noise bandwidth of 80 cps, and a VCO tuning range of ± 100 kc. The tape recorder employed will record four tracks: two data, one voice, and one time signal. The equipment is now being procured and will undergo extensive testing at GTS prior to the *Mariner C* feasibility demonstration.

D. Goldstone Operations

Preparations for installing DSIF S-band equipment, which began in mid-1963, remained secondary to the preparation for, and completion of, the *Ranger 6* operations through January 1964. From February through April the S-band equipment installation at the Pioneer Station became the primary Goldstone objective. Concurrently, operational readiness of L-band equipment was maintained at the Echo Station for subsequent *Ranger* Block III missions.

1. S-Band Construction

With the selection of the Pioneer Station as the initial installation for the operational testing of all DSIF S-band equipment and training of local and overseas personnel, it became necessary to increase the size of facilities there. An interim prefabricated building (Fig. 1) was erected to house the S-band equipment and to allow equipment testing to proceed on schedule.

Construction of the two wings (Fig. 2) on the present control building, G-1, began in late March. The east wing will house the permanent S-band equipment.

2. Equipment Installation

Pioneer Station. Two systems are currently installed at the Pioneer Station, the original L-band receiver and the new standard S-band:

(1) The original L-band receiver has been converted to L/S-band. Associated with this L/S receiver is an L/S-band transmitter that provides the required transmission capability. The original Pioneer L-band receiver was used to operationally test the L/S-band conversion of the Woomera receiver by substituting portions of the Woomera receiver into

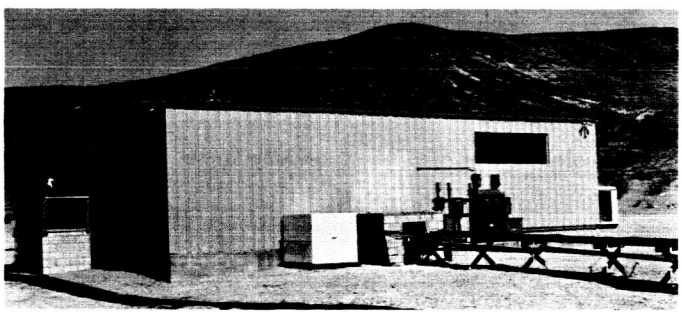


Fig. 1. S-band interim building

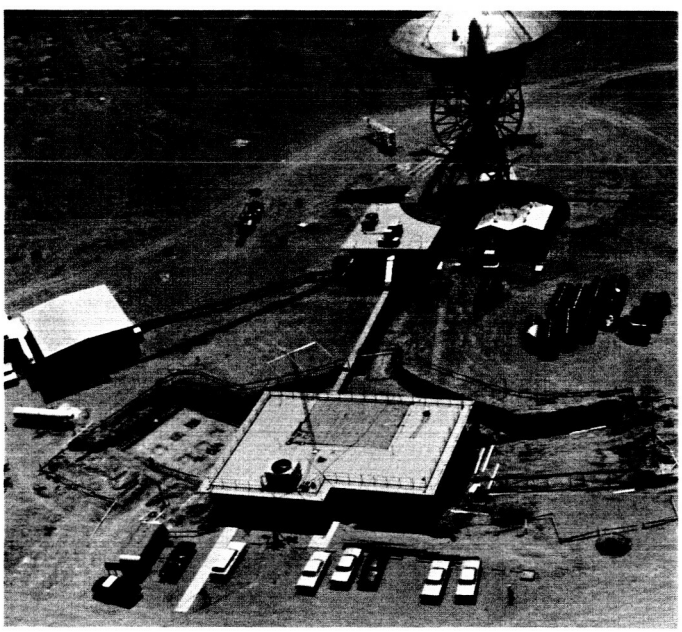


Fig. 2. Excavation for wings to control building, looking south

the Pioneer receiver; upon completion of the tests, the tested S-band components were shipped to Woomera. The conversion provides the overseas stations with the capability of either L- or S-band tracking. The Pioneer receiver has been restored to its L-band configuration and currently is being maintained in operational readiness for *Ranger 7*.

(2) The second system is the standard S-band. The receiver operates at 2295 Mc, with a dual-channel capability of receiving two spacecraft signals simultaneously. The DSIF/GSDS S-band transmitter differs from earlier transmitters in that the exciter has been incorporated with the S-band receiver. This feature provides for grouping of operating controls into a centralized position, allowing closer coordination of transmitter and receiver functions. Fig. 3 is a simplified block diagram of the major subsystems of the S-band transmitter.

The frequency and time standard signals are provided by a rubidium frequency standard, with a standby rubidium frequency standard as backup. This accurate 1-Mc frequency is coupled into a synchronizer which in turn is coupled to a frequency synthesizer. The signal from the synthesizer is then coupled into one of three variable control oscillators for accurate frequency reference. A portion of the oscillator signal is returned to the synthesizer where it is phase-locked to a zero static-phase error, resulting in a highly accurate and stable fundamental signal frequency.

The signal from the variable control oscillator is then coupled into the exciter chain. (Fig. 4 shows the exciter control panel located at the receiver–transmitter control desk.) Approximately one-half of this chain is located with the receiver, while the remainder is located in the transmitter cage on the 85-ft antenna. (Fig. 5 shows the transmitter components which are T-frame mounted in the receiver racks.) Here the signal is multiplied from the fundamental frequency to the final output frequency of 2115 Mc and is coupled into the input of an EIMAC 4KM5OSI, four-cavity klystron mounted in the antenna cage below the Cassegrain cone. The klystron high-voltage power supply is located in the hydromechanical building, and the heat exchanger is located near the base of the antenna structure. The klystron is capable of 17 kw output, but is normally operated at 10 kw continuous wave, and can be amplitude, frequency, or phase-modulated.

Associated with the standard S-band equipment is an S-band acquisition aid antenna system (Refs. 4 and 5).

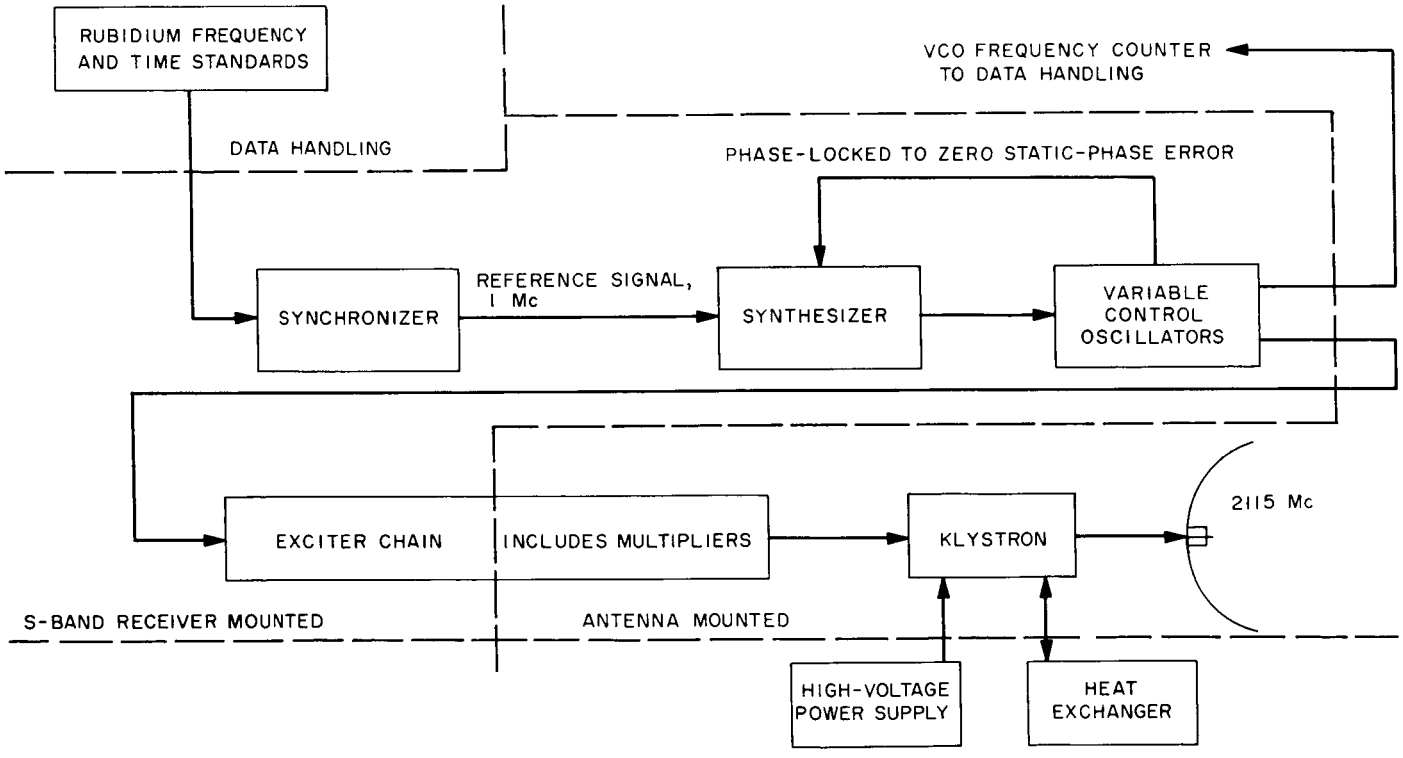


Fig. 3. S-band transmitter block diagram

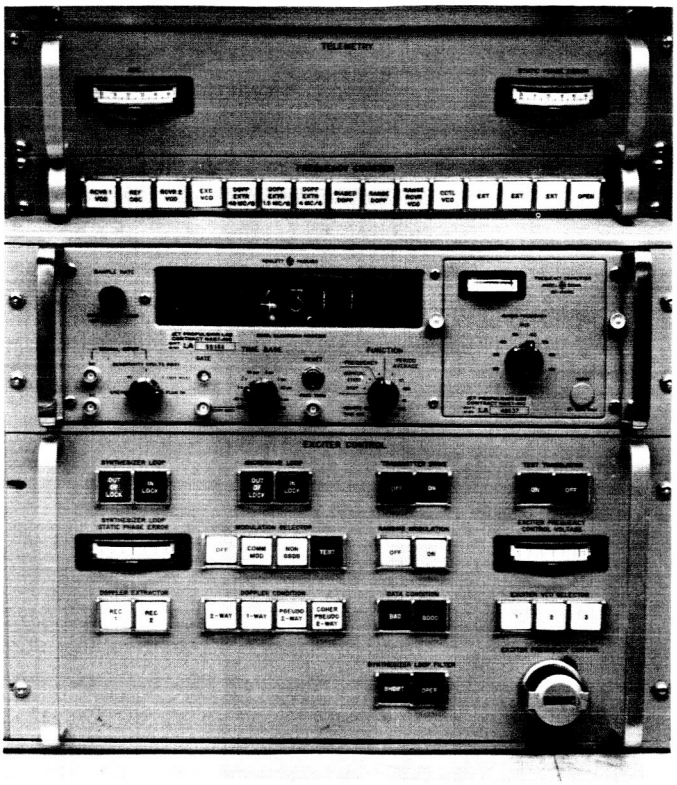


Fig. 4. Transmitter exciter control panel

Mounted on the 85-ft antenna (Fig. 6), it provides a broad beam for initial acquisition of the spacecraft. Alignment and testing of the acquisition aid antenna is performed using a folding collimation tower (Fig. 7) installed near the southeast edge of the 85-ft antenna base pad.

Installation of the standard S-band equipment in the interim building is completed and equipment testing is in progress. The installation is designed to provide a fully operational control room and a mission equipment test area. Here, prior to being sent overseas, the S-band system is operationally tested to ensure its meeting subsystem and system specifications. The general equipment arrangement is shown in Fig. 8, and four views of the control room are shown in Figs. 9, 10, 11, and 12.

The S-band Cassegrain cones and hyperbolas for the Johannesburg and Woomera Stations were tested on the Pioneer antenna, while those for the Canberra Station were tested on the Echo antenna. The Pioneer 85-ft HA–Dec antenna, equipped for S-band tracking, is shown in Fig. 6.

The standard S-band system incorporates a traveling wave maser/closed cycle refrigerator (TWM/CCR;

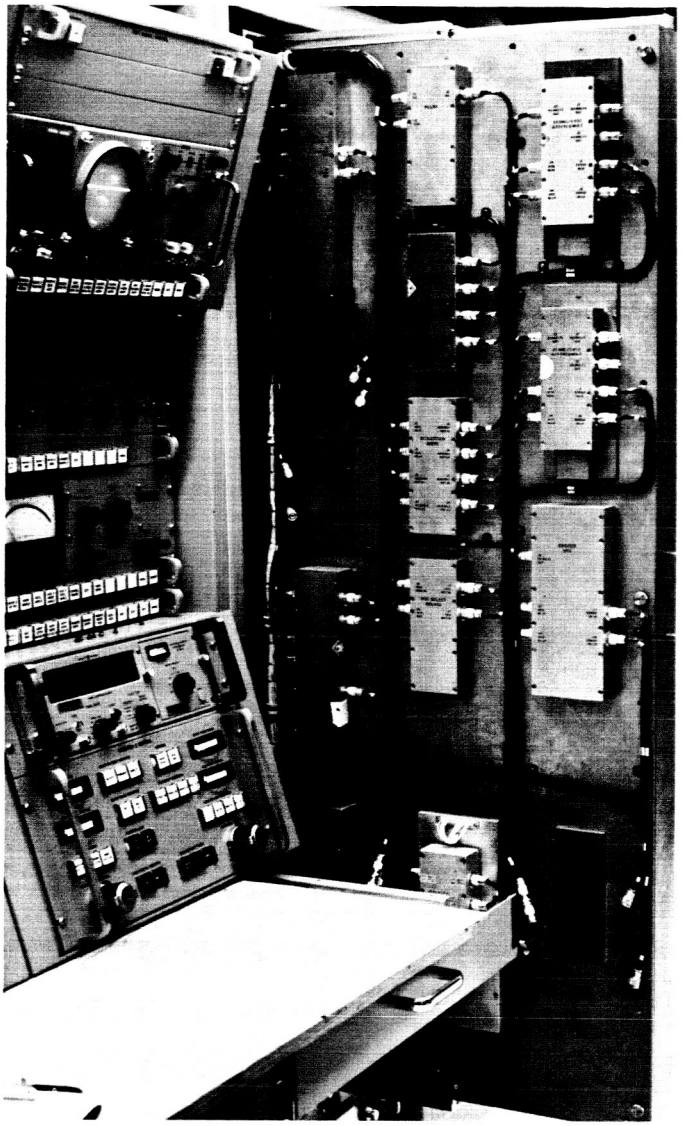


Fig. 5. Transmitter subsystem T-frame in receiver

Ref. 6) which is installed and currently undergoing operational testing. Maser personnel from Goldstone and the overseas sites attended a 2-wk school at Goldstone in March. This course was conducted by personnel from JPL and the A. D. Little Co., and covered the operation and maintenance of the TWM/CCR. Fig. 13 shows the maser assembly installed in the S-band cone on the Pioneer antenna.

Ancillary subsystems, which have been modified for and installed in support of the S-band system, include a data handling subsystem for tracking data handling and angle encoding, and an analog instrumentation subsystem with associated magnetic tape, and oscillograph recorders. Mission dependent (*Mariner C*) ground telem-

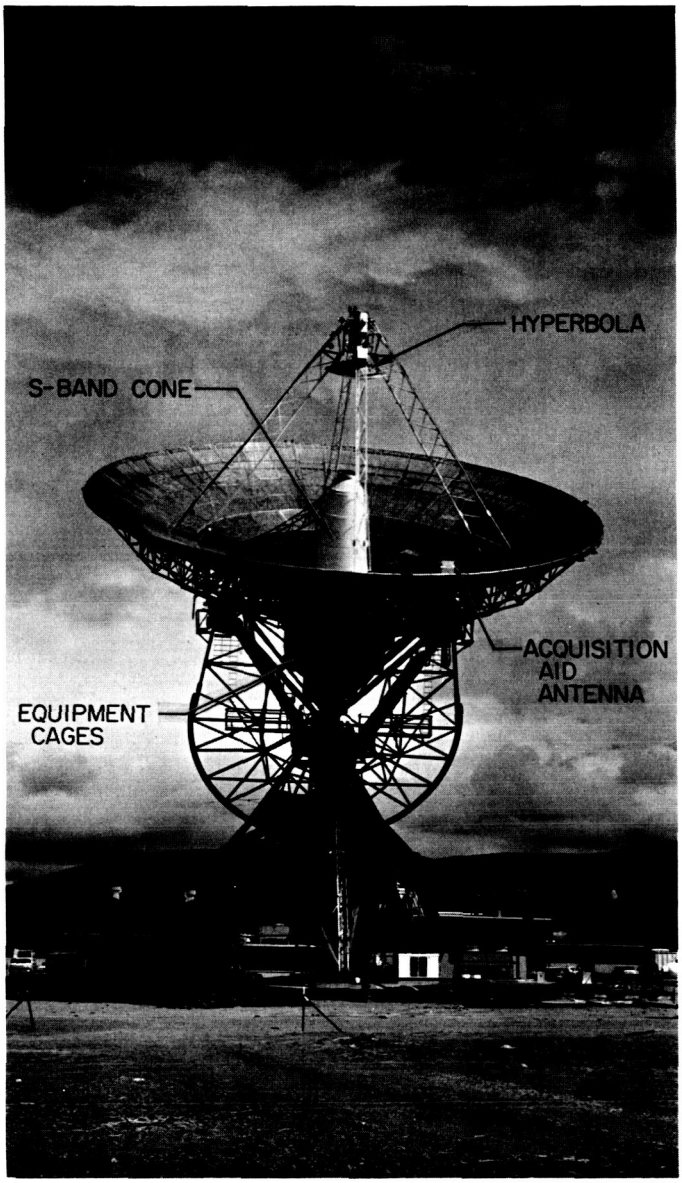


Fig. 6. Pioneer antenna rigged for S-band tracking

etry equipment is installed and is being operationally tested. Also, an Astrodata read, write, and verify ground command subsystem, capable of providing both stored and real-time commands to either *Ranger*- or *Mariner*-type spacecraft, is being operationally tested for interface agreement with associated subsystems.

The first digital instrumentation system unit (Ref. 7) has been operationally tested with the S-band equipment, and is being prepared for return to the Scientific Data Systems Co. for updating prior to its being installed at Pioneer. The second unit is installed in the S-band

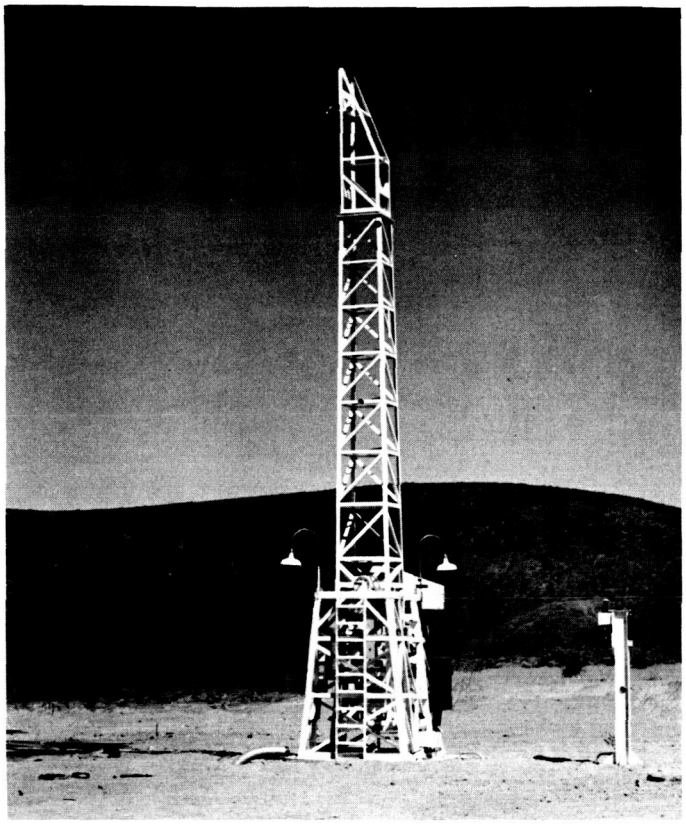


Fig. 7. Acquisition aid collimation tower

interim building and is receiving a complete program evaluation and operational interface testing.

Personnel from Woomera, Canberra, and Johannesburg are at Goldstone assisting in the installation and testing of the S-band equipment. Participation in the installation includes training in the operation and maintenance of the equipment and subsystems for which they will have responsibility at their respective sites.

Echo Station. The majority of technical personnel at the Echo Station is assisting in the S-band installation and receiving training in S-band operation and maintenance. Operational readiness of the L-band equipment is being maintained as required. Increased emphasis on preparation for *Ranger 7* will begin with the approach of the net integration and operational readiness tests. Participation in the Space Flight Operations Facility (SFOF) training tests, which began in April, currently involves the Echo instrumentation group.

The L-band receiver has had new control panels installed and tested. Minor rearrangements of subsystem

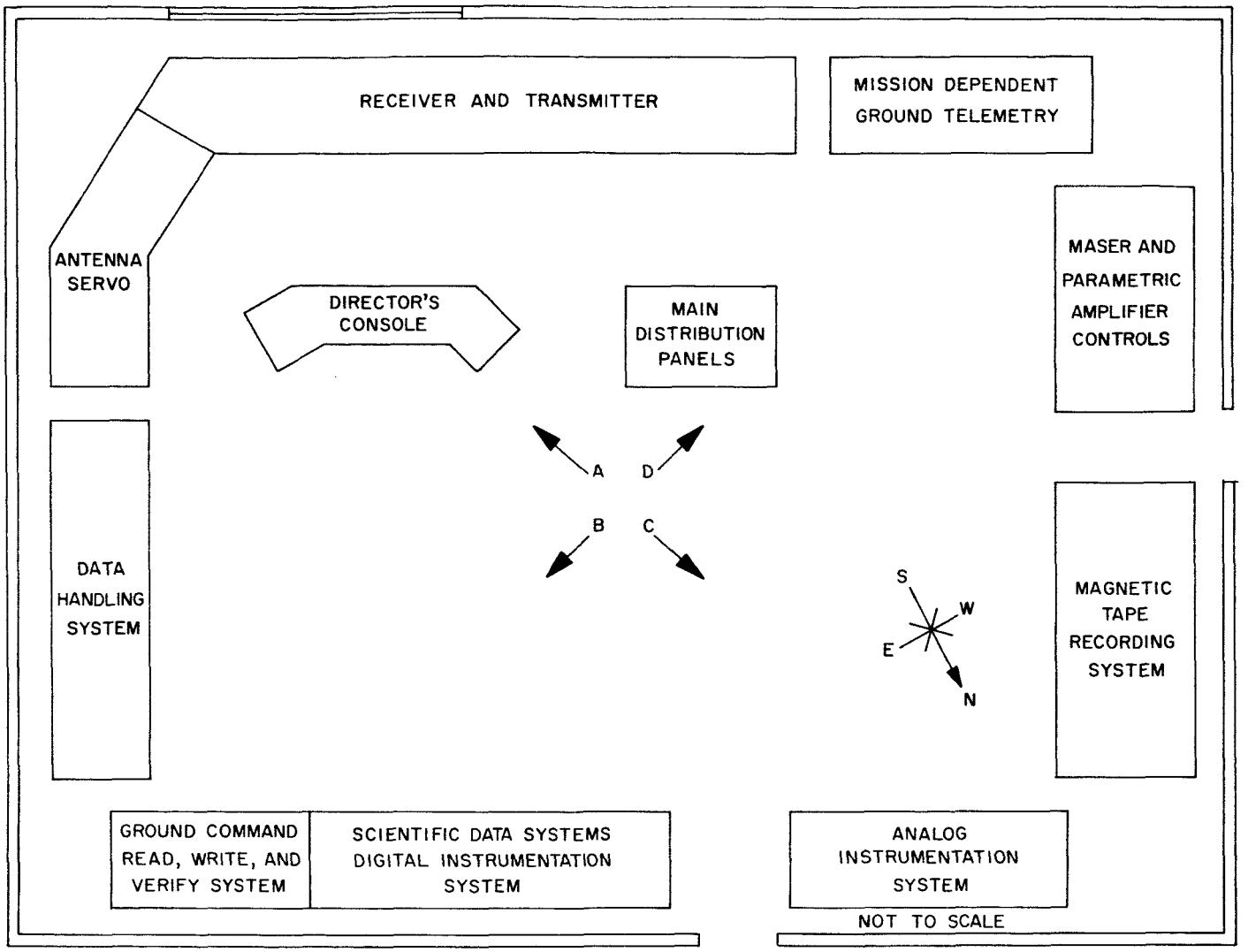


Fig. 8. Arrangement of equipment in S-band interim building

rack mounts have been made to improve ease of accessibility and control. Gain measurements were performed on the stripline mixer and the 30-Mc isolation/distribution amplifier (Ref. 8) to determine a more accurate signal level available to the RCA video equipment. These measurements and final adjustments resulted in a signal level, available to RCA, of 37 $\pm$2.0 db above the signal input to the DSIF maser.

Electro-Mechanical Research, Inc. discriminators were installed in the ground telemetry equipment, replacing the discriminators used during *Ranger 6*. The new discriminators have been operationally checked in a series of tests with JPL and indicate a higher degree of reliability. The Astrodata read, write, and verify ground command subsystem received minor modifications which have improved circuit reliability and control functions.

3. Surveyor Program

Personnel and equipment from Hughes Aircraft Co. have arrived at Goldstone. The *Surveyor* ground equipment for the Goldstone installation is being installed in the Pioneer control building. Essentially, it consists of ground telemetry and video control and monitoring equipment which will be used during the *Surveyor* flights and after the landing on the Moon's surface.

4. Goldstone Area Map

A map of the Goldstone area, showing the new building additions at each station, is shown in Fig. 14.

Fig. 9. Control desk area of receiver and transmitter

Fig. 10. Data handling and digital instrumentation systems

Fig. 11. Analog instrumentation system

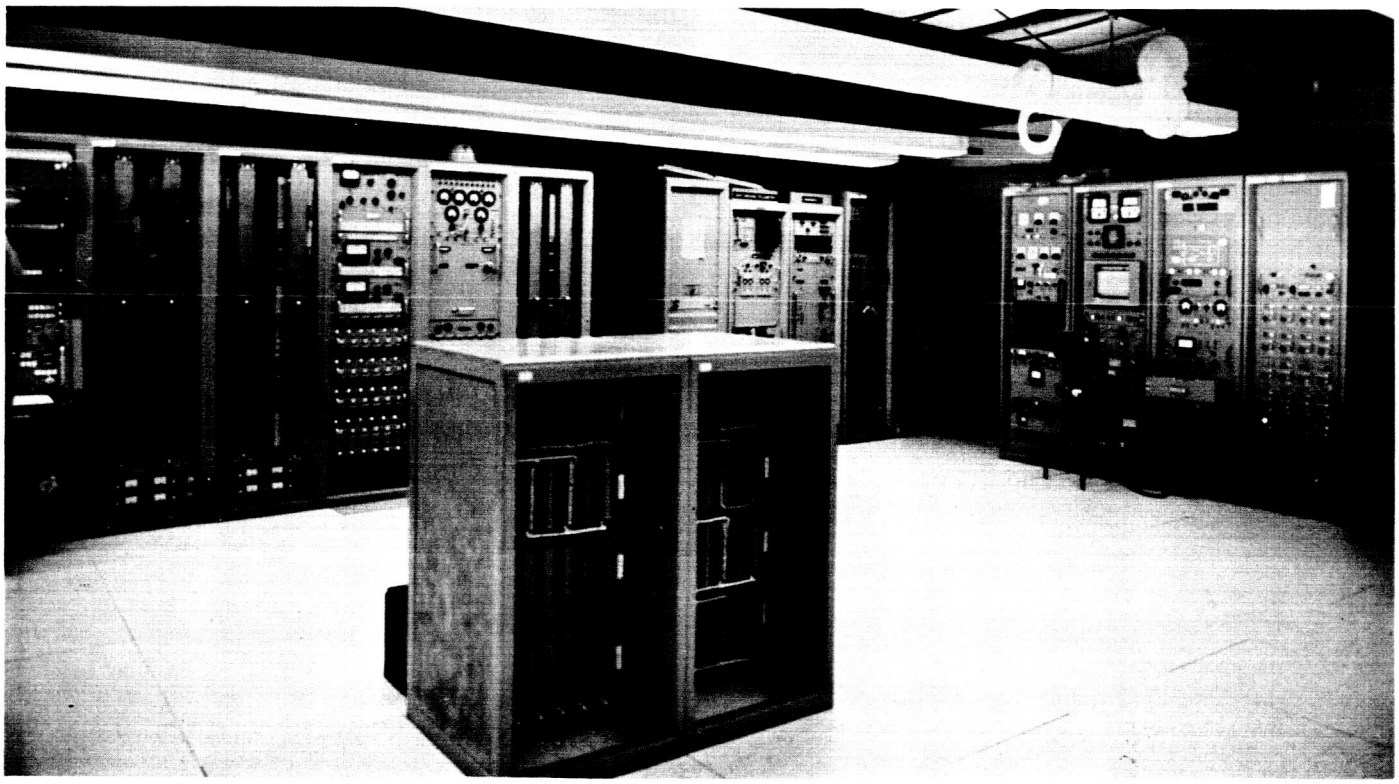


Fig. 12. Maser and parametric amplifier control and ground telemetry

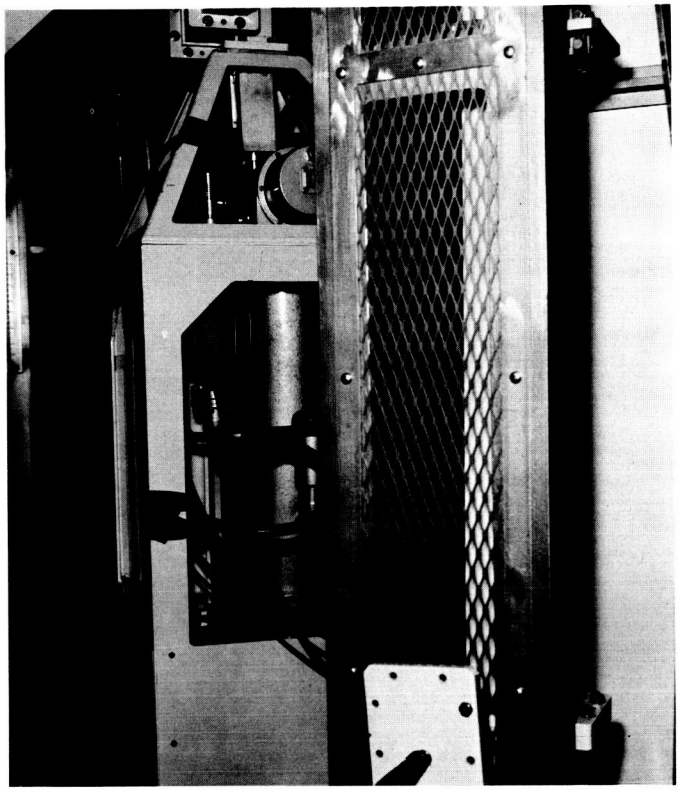


Fig. 13. TWM/CCR in antenna cone

E. Antenna Engineering

From September 1, 1963 to March 15, 1964 various modifications and additions were made to the Pioneer Station antenna to prepare it for S-band operation.

These modifications and additions cover five general areas: retrofit structural modifications, optical tracking aid system modifications, S-band acquisition aid support hardware installation, 85-ft dish resurfacing, and final alignment. These areas are briefly discussed here.

1. Retrofit Structural Modifications

The retrofit modifications comprised seven items and included the removal of the old dish structure electronics cages and tubular quadripod.

Declination wheel electronics house. A two-level weatherproof electronics house was constructed in the previously existing void in the declination wheel structure (Fig. 15). This house is to afford space for the increased amount of S-band electronics requiring mounting in the antenna; such space must be weatherproof, capable of being air conditioned, and possess integral service hoisting capabilities.

The mounting of this large facility in the declination wheel structure not only aids the declination wheel counterbalancing situation by placing the electronic module weight in an advantageous location, but also allows the removal of the electronics and transmitter cages in the dish structure.

The declination wheel house supplies a total usable volume of 1815 ft^3 and 220 ft^2 of floor space.

New declination axis bearings. Here the existing declination axis bearings (having excessive radial and axial tolerances up to 0.050 and 0.150 in., respectively) were replaced with better quality bearings (Fig. 15) of improved tolerances (having radial tolerances less than 0.015 in., and axial tolerances less than 0.030 in.).

This modification was made not only to improve pointing and tracking capabilities but to prevent a failure of the encoding readouts caused by rupture to the couplers due to excessive declination shaft movements.

New truss-type quadripod. The old tubular-type quadripod was replaced with a truss type (Figs. 16 and 17) of improved strength and stiffness.

This modification was made necessary by the addition of the S-band hyperbola assembly and the allowable S-band quadripod deflections with their attendant effects on pointing and tracking capabilities.

Hour angle and declination counterweight cages. Because of the above and other planned additions such as the environmental subsystem, Cassegrain subsystem, S-band acquisition aid subsystem, etc., the existing counterweight cages had insufficient capacity. The new cages have enough capacity to handle all planned additions plus a 10% growth capability. Also, the cages are mechanized for easier addition of lead and in smaller pieces (Fig. 15). When all hardware has finally been installed, the antenna balance will be measured and the antennas properly balanced so as not to degrade the maximum drive rate capabilities.

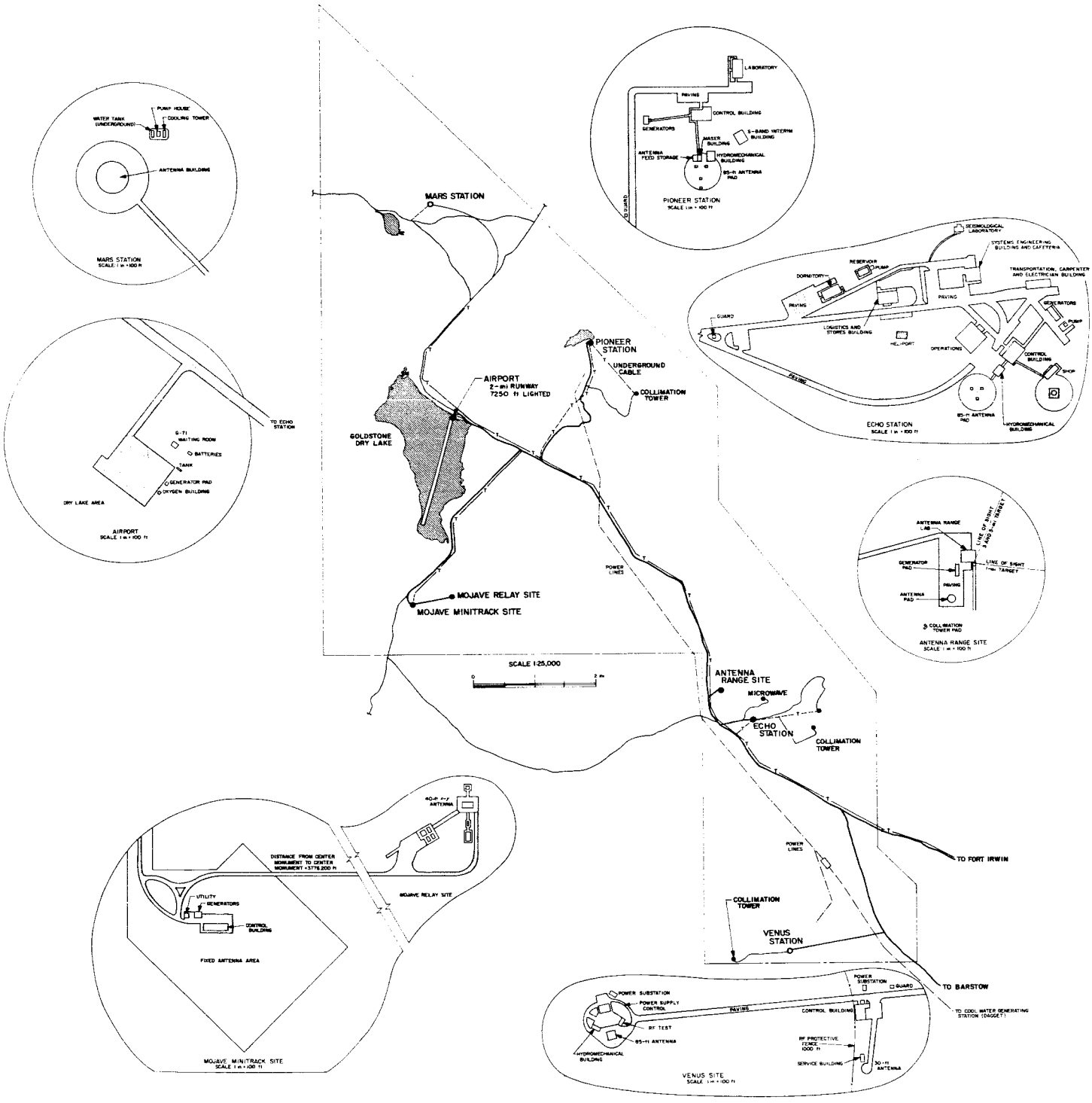


Fig. 14. Goldstone area map

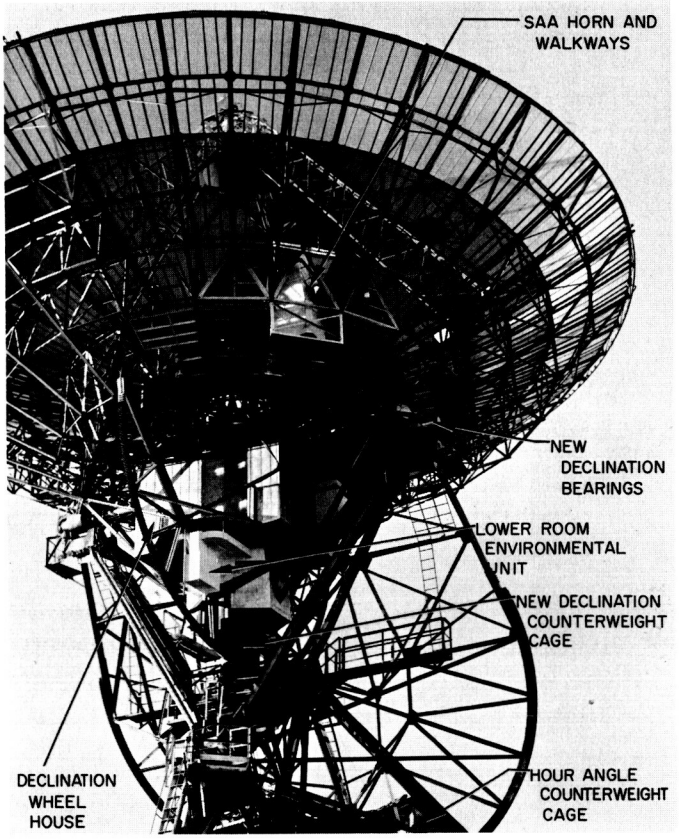


Fig. 15. Pioneer antenna supporting structure

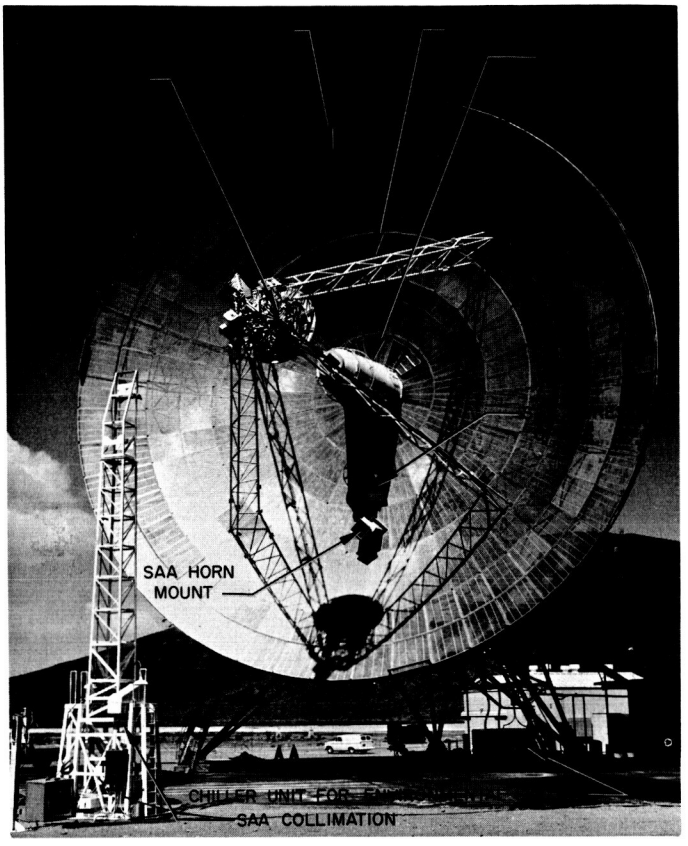


Fig. 16. Pioneer antenna reflecting surface and quadripod

Structural beefup. Because of the retrofit additions, it was necessary to increase the area of certain primary members and to add members in the declination wheel area in order to maintain the level of strength and stiffness existing prior to the additions and modifications.

A computer check using the structural analysis interpretive routine (STAIR) and stiffness matrix programs was run to determine that the antenna's strength, stiffness and basic frequencies, as well as pointing and tracking capabilities existing prior to the work, were maintained or improved.

Cassegrain subsystem modifications. This was the replacement of the existing L-band Cassegrain cone and hyperbola with an improved S-band Cassegrain cone, one sheeted with 7178-T6 aluminum and painted with JPL's new paint system (Figs. 16 and 17).

The hyperbola and backup structure are the improved S-band configurations with the new position readout hardware and laminated hyperbola of 7178-T6 aluminum which affords hailstorm protection, reduced weight, and improved surface accuracy (from 0.125- to 0.031-in. rms; Figs. 16 and 17).

Environmental control system. The environmental control system modification consists of the addition of a chiller unit (10-ton capacity) located at the northeast leg of the antenna pedestal (Fig. 16) and three heat exchanger units in the antenna.

The exchanger units are for the lower room of the declination wheel electronics house, the upper room, and the Cassegrain cone. The units have sufficient capacity to maintain the temperature of each specific area at 70 $\pm 10°$F under all expected operational conditions. Fig. 18 is a close-up of the exchanger unit for the Cassegrain cone.

2. Modified Optical Tracking Aid (OTA) System

The existing OTA systems on the Pioneer and Echo antennas have been overhauled and modified:

(1) Bases of the TV and boresight cameras and lens mounts have been modified for the new snap-in

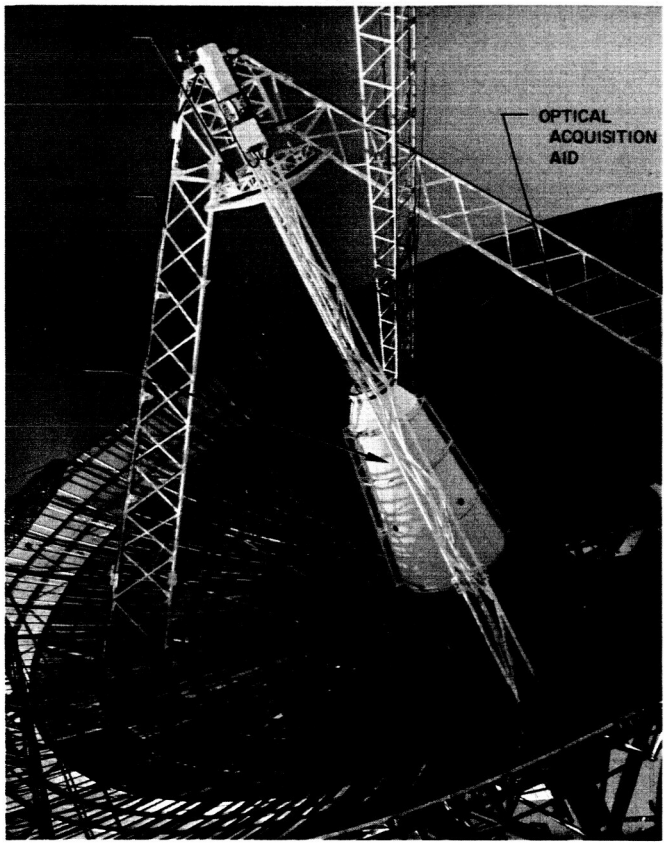


Fig. 17. Pioneer antenna Cassegrain cone and quadripod structure

Fig. 18. Cassegrain cone environmental unit

mounts which afford quick camera removal for servicing or switching, eliminating the previous long time period requirement for camera realignment.

(2) The filter wheel drive mechanisms have been modified, replacing the old stepping switch drive with a dc motor drive. The new drive affords more positive filter positioning and removes the previous susceptibility to jamming caused by filter wheel case misalignments or bending.

(3) Cabling from the antenna optical package to the control room has been changed from one to several cables. The new cables are routed through junction boxes at the antenna end to permit servicing of either the TV or boresight camera (BC) without disabling one or the other.

(4) The TV controls, TV filter wheel, and automatic door cover controls have been separated into two modular assemblies to improve reliability, system noise level, and field servicing.

(5) The BC control unit (Fig. 19) has been modified to provide for the following items, so that said events are indicated and any failures or nonoperating status are immediately identified:

Self-indicating fuses.

Film progress frame counter.

Film supply meter.

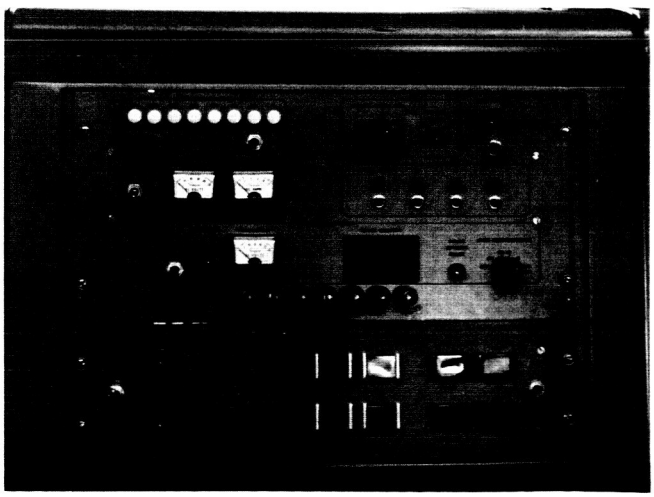


Fig. 19. Boresight camera control and SAA collimation tower control unit

Reticle power light.

Frame advance and film take-up light.

Code lamp operational lights.

3. S-band Acquisition Aid (SAA) Support Hardware

In support of the SAA system, the following hardware items were developed and installed at the Pioneer Station.

Optical acquisition aid (OAA) subsystem. This is a TV camera-lens system (Figs. 17 and 20) similar to the main OTA system, enabling the servo operator either to boresight the SAA horn on its collimation tower (Fig. 16) or to track a target such as a helicopter. The system comprises a reference telescope, TV camera and monitor, and a 4-deg field of view *f*2.5 lens (Figs. 16 and 17).

SAA horn mounting hardware. This includes the mounting hardware for positioning and holding the SAA horn in the antenna dish structure and the associated service walkways (Figs. 16, 17, and 21).

SAA servo control unit. This affords the link between the SAA horn end signals and the servo system as follows:

The Goldstone duplicate standard (GSDS) servo system has been supplemented with the necessary control and switching circuits for accepting error signals from either the S-band acquisition or tracking receivers. Provision for switching has been made for both the pure S-band and L/S-band configurations. The necessary switching and control circuits are manifested in the acquisition aid servo control console, item 060709 on the DSIF

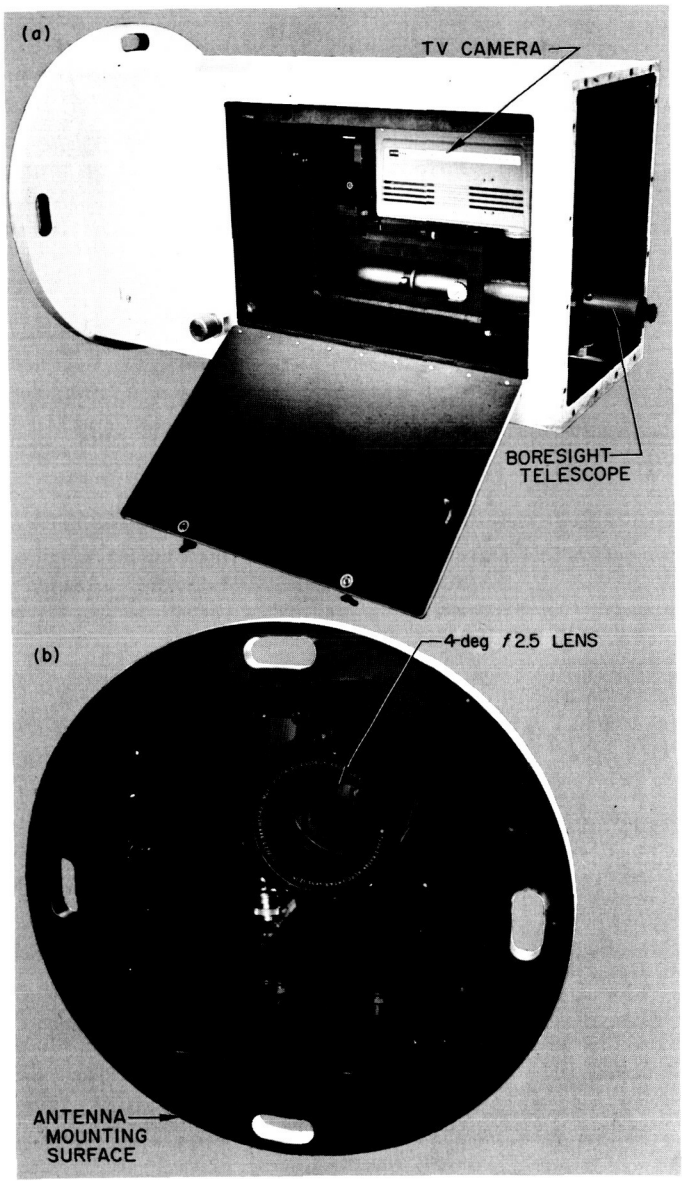


Fig. 20. SAA optical package

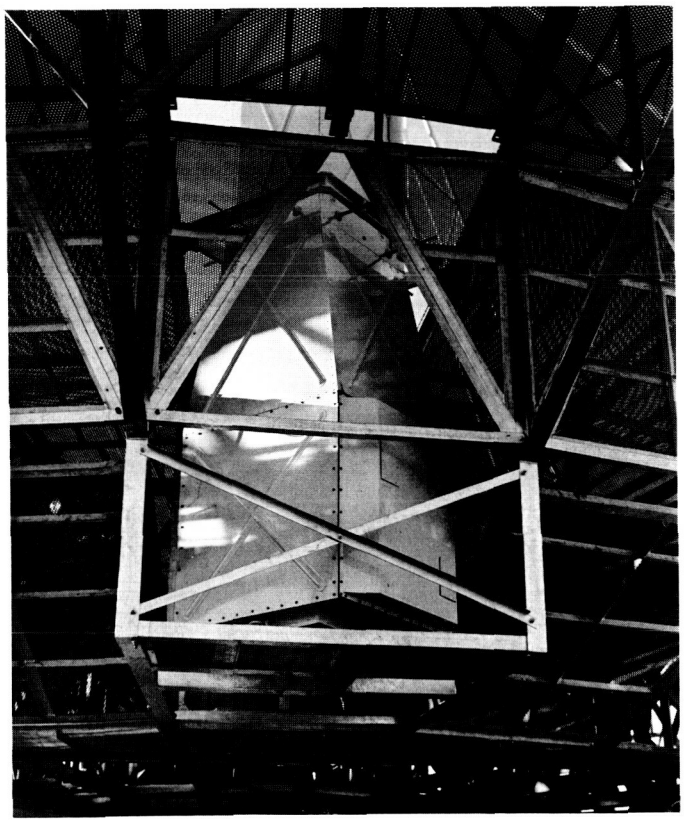


Fig. 21. SAA horn and walkways

block diagram and located in console 4 of the standard DSIF control room layout. The control circuitry which comprises this console consists primarily of necessary relay contacts and an adjustable gain, operational amplifier which compensates for the difference in gain between the acquisition aid and normal tracking receiver systems, thus maintaining a constant tracking loop gain. Block diagrams for both the L/S-band and pure S-band systems are shown in Figs. 22 and 23. The control panel for the S-band block is shown in Fig. 24.

The design philosophy for this signal processor involves affecting the switchover between the acquisition and tracking receivers with a minimum switchover transient. The switchover is accomplished in this manner:

Acquire and automatically track in the acquisition mode.

Zero the error in the normal narrow beam tracking receiver by means of the bias input.

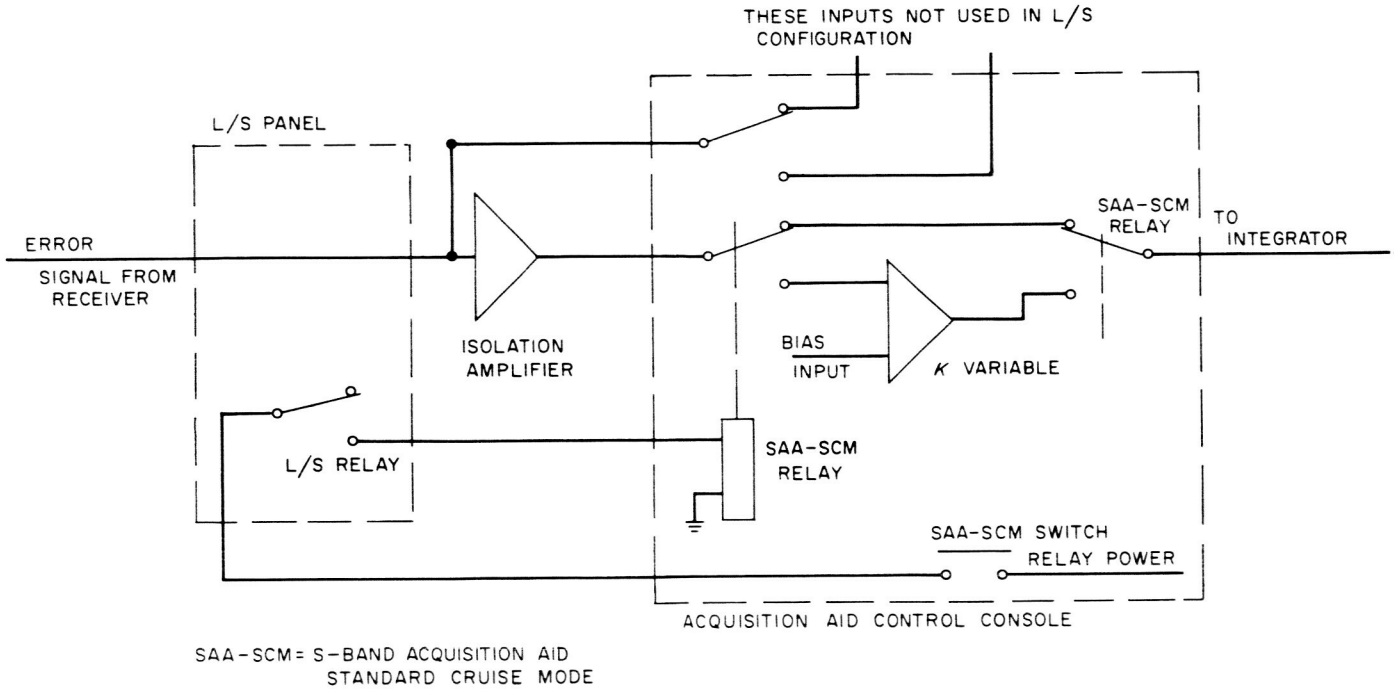


Fig. 22. Acquisition aid control for L/S-band system, block diagram

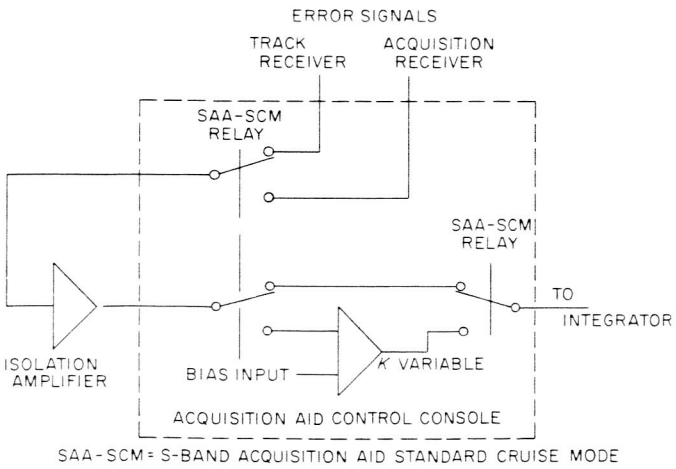


Fig. 23. Acquisition aid control for S-band system, block diagram

Fig. 24. SAA control panel

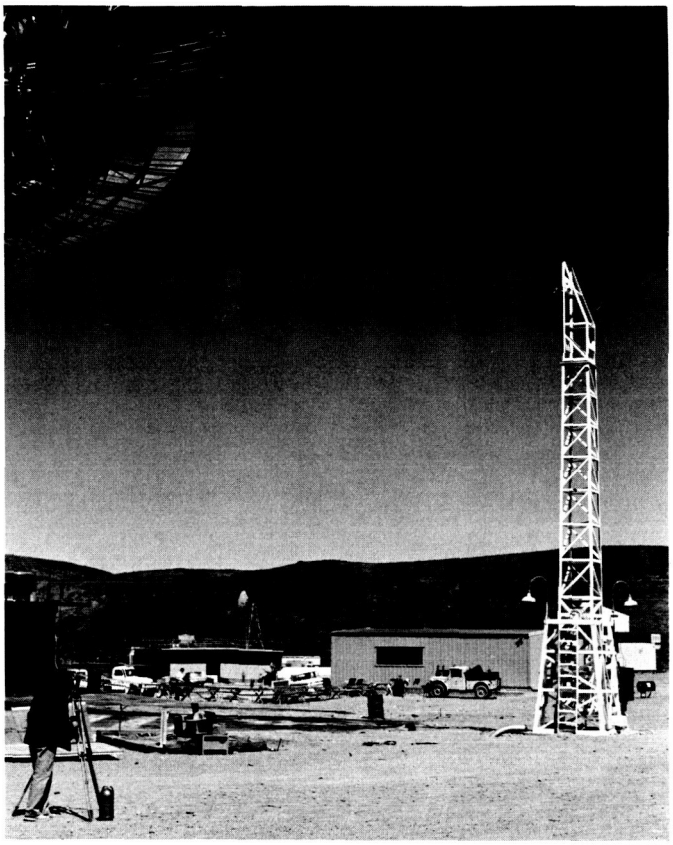


Fig. 25. SAA collimation tower in elevated position

Switch from the acquisition to the normal narrow beam tracking mode.

For the L/S-band interim system, it was decided to use the same console as for the pure S-band signal processor and add a small chassis which would provide the necessary interface connections between the S-band servo system and the L-band receiver, thus conserving console space and reducing redundancy. The circuitry contained in this interface panel provides for processing the incoming error signal from the L-band receiver, modified for S-band operation, and for actuating the waveguide switches on the antenna. This small panel is expendable, thus allowing its disposal when the DSIF no longer uses the L/S-band receiver system.

SAA collimation tower. A 30-ft-high remote controlled collimation tower was supplied for the Pioneer SAA system (Figs. 16, 25, and 26). The tower can be raised and lowered to a specific position with a repeatability of 0.050 in. or less in a 35-mph wind, to less than 0.100 in. in a 60-mph wind, and will survive in its lowered position, in tolerance, a 120-mph wind.

The tower normally carries an RF boresight horn in its upper cage. Fig. 19 shows the remote control panel. The tower may be raised or lowered automatically, from the servo operators console position to a locked position, or manually in specific steps.

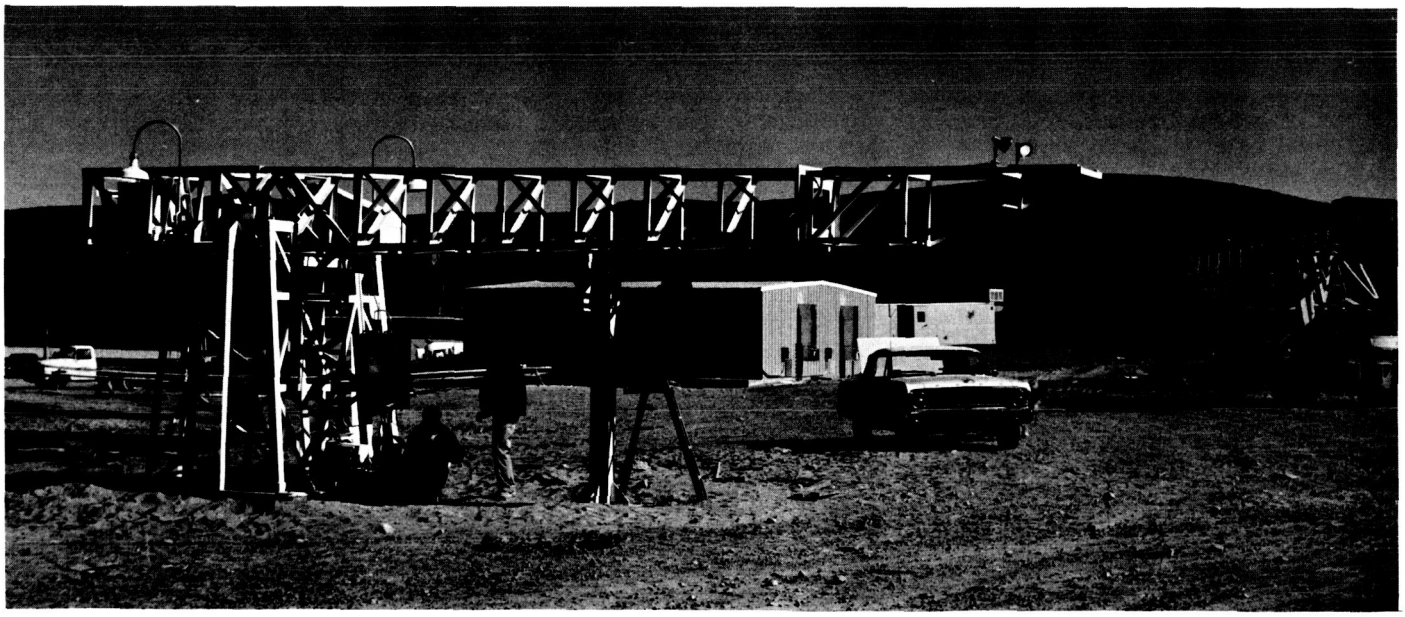


Fig. 26. SAA collimation tower in retracted position

4. Resurfacing of Pioneer Antenna Dish

The surface of the Pioneer dish (i.e., the expanded aluminum mesh portion) has suffered extensive damage; therefore, it was repaired by replacing the inner 75% of the radii with a 6061T6 aluminum sheet having 25% porosity, 0.375-in. holes, and an 0.080-in. thickness. The outer 25% of the radii was repaired with similar sheeting but of 50% porosity.

This new skin affords an improvement in the previous surface tolerances of approximately 2 (from approximately 0.25 to 0.125-in.) and improvement in noise temperature of approximately 4°K (or more) and an improved resistance to possible damage resulting from walking, dropped tools, hailstorm, etc., with a minimum increase in wind loading.

5. Final Alignment of Pioneer Antenna

The Pioneer antenna has been given its final alignment adjustments and position measurements and the pedestal base shoes have been kirksited and grouted into place (Fig. 27).

Meridian and latitude alignments of the polar shaft have been set to better than 2 sec of arc.

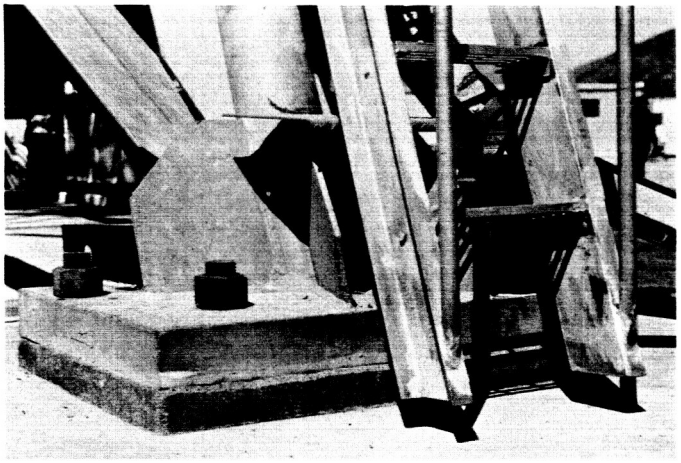


Fig. 27. Grouted antenna base shoes

F. Computer-Controlled Antenna-Positioning System

1. System Description

A computer-controlled antenna-positioning system is now being installed at the Goldstone Station Venus site. This system will be evaluated for eventual use on all stations of the DSIF tracking network. The over-all design concept was to use a small general purpose computer to handle as much of the operation as possible thereby minimizing the amount of peripheral equipment required. Factors of future expansion, flexibility, cost, and simplicity of operation were also taken into consideration.

The system (Fig. 28), when in operation, will be enclosed in the servo drive loop on an 85-ft diameter azimuth–elevation mounted tracking antenna located at the Venus site. Inputs of antenna position from the angle encoding system and GMT from the data handling system will be required. In addition, digital inputs from a system control panel will be utilized. Digital-to-analog converters will supply output voltages to the antenna servo system in proportion to the antenna position error. Outputs will be provided for the recording and display of selected functions within the computer. All control of data input–output, comparisons, calculations, error detection, and code conversions will be accomplished by the computer.

The program is now completed for the following system modes of operation.

a. Mode 0. The computer will idle in this mode. No error voltage is provided to the servo system. This will be a waiting condition until an operational mode has been selected.

b. Mode 1. This mode provides for antenna positioning from a precomputed ephemeris paper drive tape consisting of samples of time and angles. The drive tape will be read by the computer photo reader and will be pulled under computer control. Data samples on tape may have any time interval from 2 sec to several hours. The computer will perform linear interpolation between samples for continuous antenna positioning. A significant amount of tape error detection has been included in this program. Erroneous data will be disregarded and the computer will search the tape for the next valid sample to use for interpolation. Tape time and GMT synchronization is performed by the computer. A tape time pull offset may be introduced from the control panel.

c. Mode 2. This mode provides for automatic antenna positioning at Earth rate by internal sidereal clock. In this mode, a programmed sidereal clock moves the antenna at sidereal rate. The sidereal clock is updated by

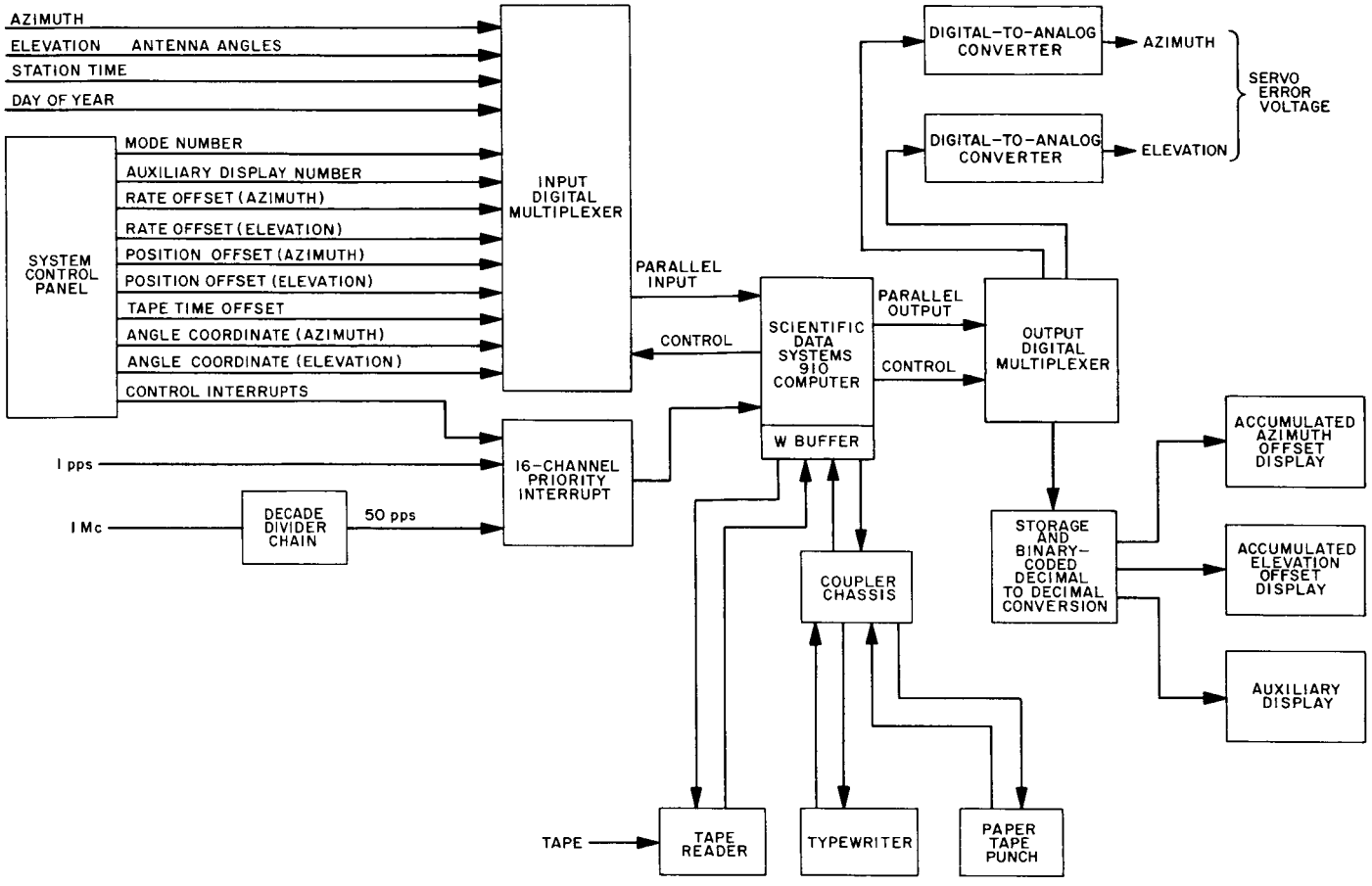


Fig. 28. Computer-controlled antenna-positioning system block diagram

use of the station GMT clock and timing interrupts. This mode is initialized by the selection of desired sidereal hour angle and declination coordinates of either stars, planets, or spacecraft on the system control panel. When this has occurred, the antenna will position to these preselected coordinates and continue its movement in local hour angle at sidereal rate. Coordinate conversion is used to transform from the polar reference coordinates to azimuth–elevation commands to position the antenna. Antenna motion may be modified by the selection of rate and position offsets from the control panel. An optional feature of this mode will be an elevation refraction correction for star tracking.

d. Mode 3. This mode provides for antenna movement to preselected azimuth–elevation coordinates. In this mode, the antenna will move to any selected coordinates (collimation tower, for example) and halt.

e. Modes 4 and 9. At present, these modes are not programmed but are available for future use. Other modes could include such tasks as trajectory calculation and positioning from parameter inputs, programmed corrections for structural misalignments, and generation of antenna search patterns.

2. System Control Panel

A system control panel (Fig. 29), fabricated by JPL, is used to direct the operation of the computer. Information is transferred from the panel to the computer by push-button interrupts actuated by the system operator. The interrupts may either command the computer to perform a particular calculation or to read digital information selected on digiswitches located on the control panel.

Selectable information includes mode number, offsets, and coordinate inputs. Data is selected in decimal form and converted to a binary format by the computer. Position offsets will range from ± 9.999 to ± 0.001 deg in 0.001-deg steps. Rate offsets may be varied from ± 0.399999 to ± 0.000001 deg/sec in 0.000001 deg/sec

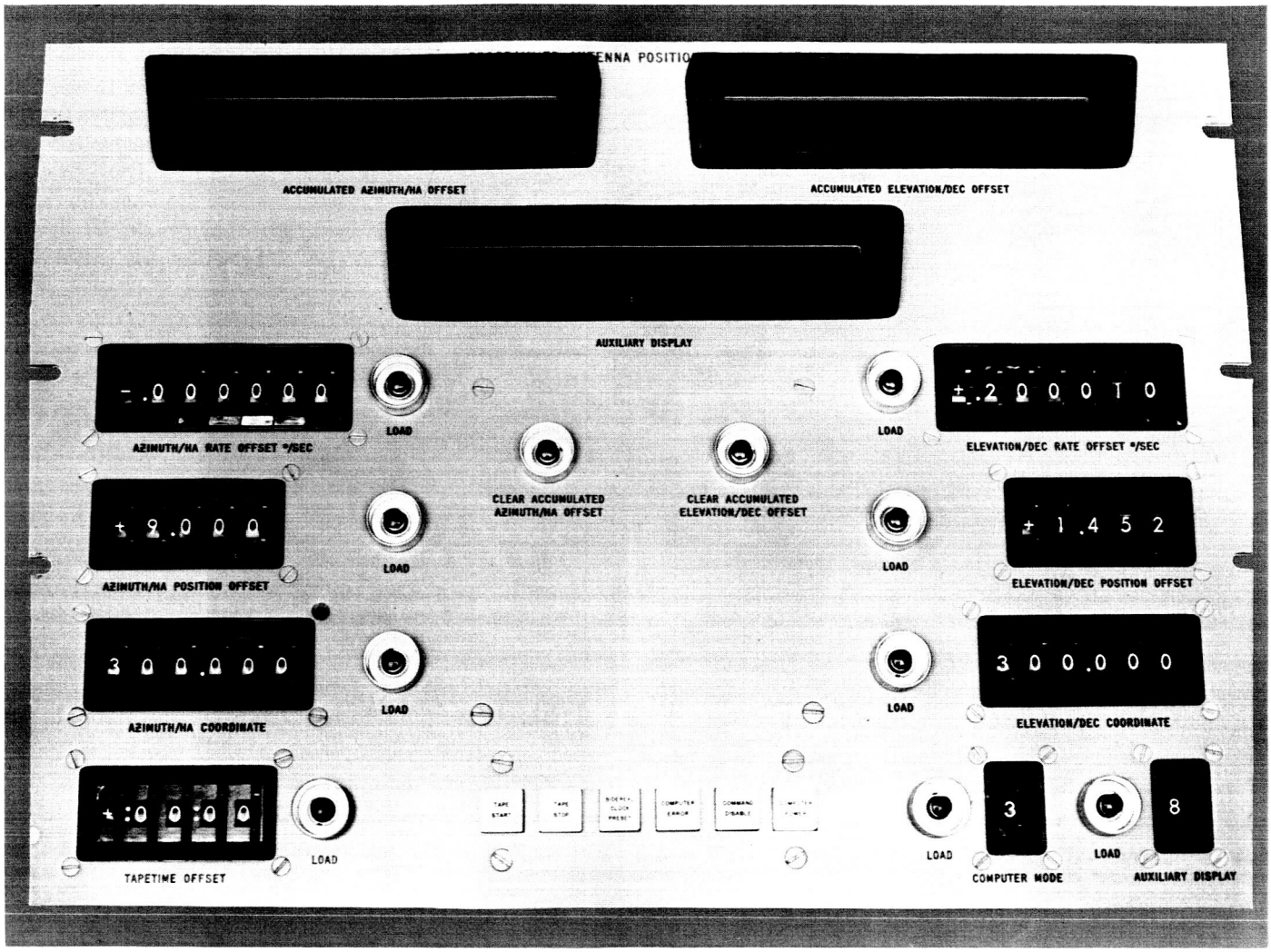


Fig. 29. Antenna-positioning system control panel

steps. Coordinate selection will range from 000.000 to 359.999 deg in 0.001-deg steps. The tape pull time offset may be changed on 1-sec steps from 1 sec to 1 hr.

Other features of the system control panel consist of such functions as: OFFSET CLEAR, TAPE START AND STOP, PRESET SIDEREAL CLOCK, and TURN ON COMPUTER POWER. Also, a computer error indicator will be turned on when the computer fails to run or when an input–output error has occurred. A master clock of 50 pps is used to interrupt the computer into an antenna position updating cycle. Accumulated offset will be continuously displayed for both antenna axes on the system control panel. In addition, a third auxiliary display will be capable of displaying any one of ten functions on command from a switch on the control panel.

3. Peripheral Equipment

An SDS 910 computer with 2000 word memory, paper tape punch, photo reader, and typewriter is used in conjunction with special interface equipment supplied by Scientific Data Systems Corp. A brief description of the peripheral equipment is given here.

a. 16-channel priority interrupt. A priority interrupt system will be used by the computer to receive timing signals from the station clock and commands to read inputs from the control panel.

b. Power fail safe chassis. The power fail safe chassis preserves all data in the computer registers and other volatile information upon failure of main power.

c. Input multiplexer. The input multiplexer will provide selection of 1 of 18 digital data words upon receipt of a command from the computer. A data word shall consist of 24 parallel bits of information. The selected word will be presented to the computer parallel input system. The inputs to the multiplexer will consist of:

Station time from the data handling system.

Antenna position from the angle encoding system.

Selected information from digit switches on the system control panel.

Spare channels for communication from external computers and systems.

d. Output multiplexer. The output multiplexer provides for the selection of 1 of 12 output devices connected to the computer parallel output system. The output devices of the multiplexer will be:

Three decimal displays.

Two digital-to-analog converters.

Spare channels for communication to external computers and systems.

e. Decimal displays. Three six-digit displays will be used to portray various functions in the computer.

f. Digital-to-analog converters. Two of these converters will transform 8-bit binary (plus sign) to an analog voltage. They will be used to provide the servo system with a voltage corresponding to position error.

g. Decade divider chain. A decade divider chain will be utilized to obtain computer timing signals derived from the station 1-Mc standard.

The entire system will be housed in three equipment racks. Two of these will contain the 910 computer and the third will accommodate the peripheral equipment. Provisions have been made for future expansion in all areas of the input–output equipment. The system control panel will be located on the servo system control console. The computer will have its own control panel to enable independent use for other applications during nontracking periods. In addition, a limited amount of operations may be performed on a time-share basis while the computer is performing its primary mission of antenna positioning.

G. Mark I Ranging Subsystem

The Mark I ranging subsystem is being built to equip the DSIF with the capability of ranging on spacecraft "turnaround" transponders to distances of 800,000 km. A summary of the basic theory of operation and a brief over-all description of the subsystem were given in Ref. 9. The design and operation of the major functional units were further detailed in subsequent volumes of *SPS*.

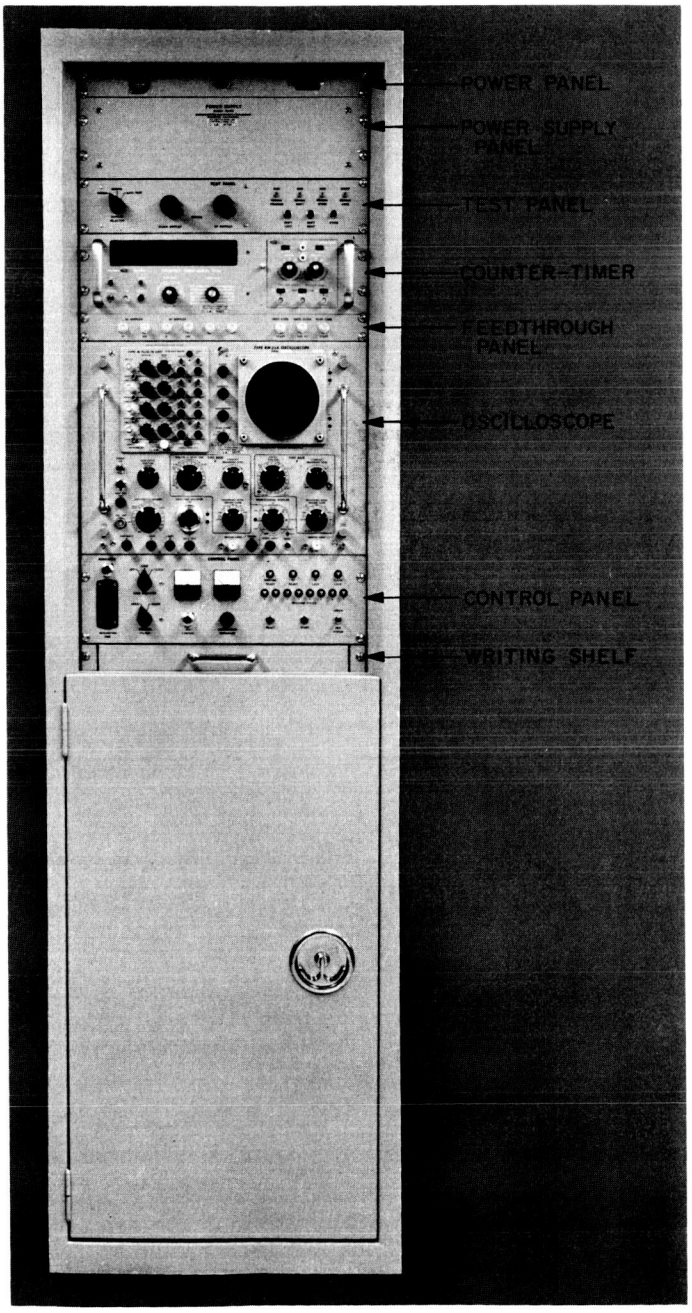


Fig. 30. Mark I ranging subsystem, front view

In this summary the project progress and current status are presented.

Design of the Mark I ranging subsystem has been completed and a prototype has been built for laboratory use. This prototype has been mated with the S-band test receiver–transmitter at JPL. Helicopter transponder ranging tests have been run, using the now obsolete *Ranger* follow-on S-band transponder prototype and the now current *Mariner C* transponder prototype. These tests confirmed the completeness and accuracy of the design of the ranging subsystem whose performance was found to be essentially identical with that of the experimental Mod II system described in Ref. 10.

Construction of the Serial No. 1 (Pioneer) subsystem has been completed, and construction of Serial Nos. 2, 3, and 4 is in progress. Fig. 30 is a front view of the subsystem cabinet. The bottom portion, behind the door, houses the digital modules which comprise the bulk of the subsystem. The visible panels, starting from the top, are:

Power panel. This panel contains a circuit breaker (which also serves as the subsystem power switch), a subsystem power indicator lamp, and a running time meter.

Power supply panel. This panel contains various power supplies and has no front controls or indicators.

Test panel. The functions performed by this panel (Fig. 31) were reviewed in Ref. 11. The appearance of the panel has been changed and some of its former functions have been removed; the remaining ones are

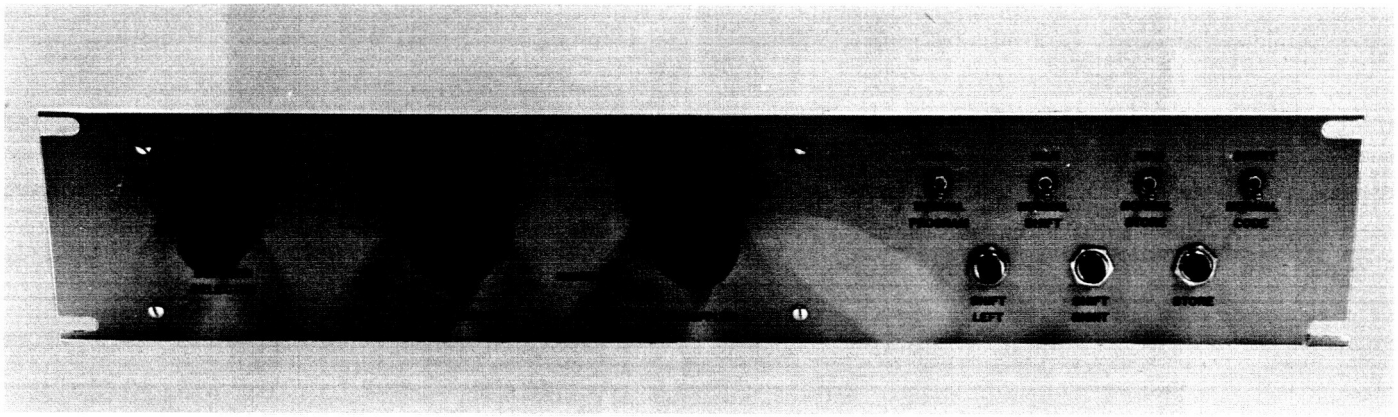


Fig. 31. Mark I ranging subsystem test panel

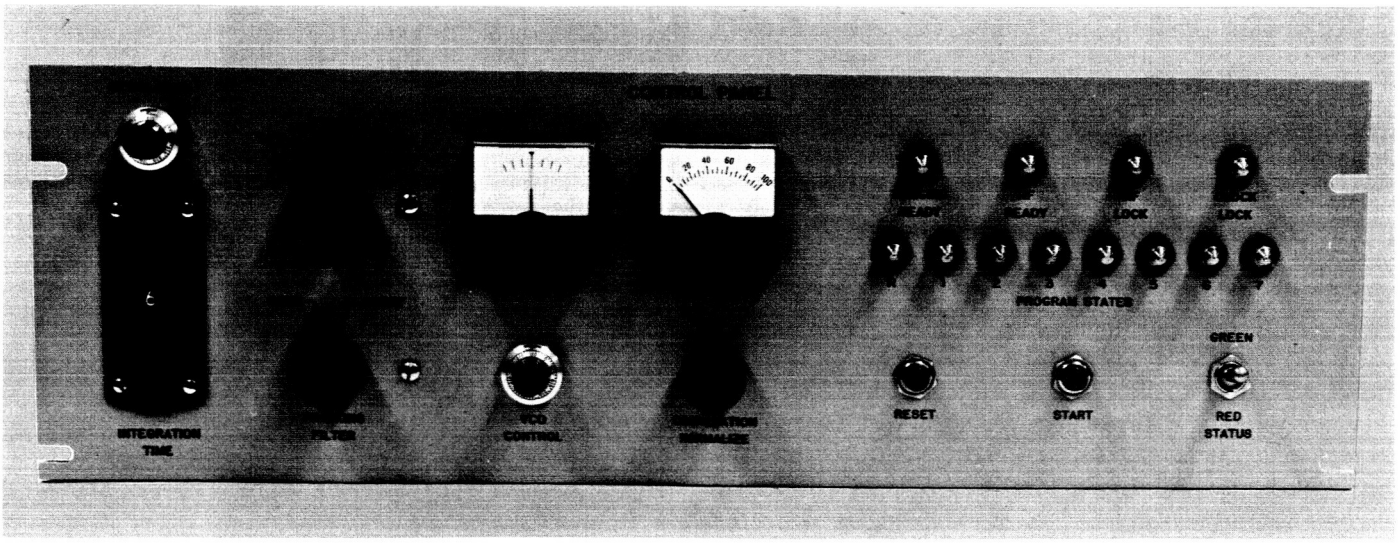


Fig. 32. Mark I ranging subsystem control panel

as described previously. The functions removed have been incorporated into the radio system simulator and the data system simulator. These test units will be described here; they are not integral with the subsystem.

Counter–timer. This device is primarily test equipment; it is used incidentally to provide a range display for monitoring by the operator.

Feedthrough panel. This panel provides convenient access to signals most often used with the counter–timer and the oscilloscope.

Oscilloscope. This test equipment has a four-trace preamplifier and a calibrated delayed sweep feature; it is essential for subsystem checkout and troubleshooting.

Control panel. The function and appearance of this panel (Fig. 32) remain essentially as described in Ref. 12. The major change is the addition of the control marked MODULATION which varies the amplitude of the transmitter code signal supplied to the transmitter and hence varies the transmitted signal modulation index.

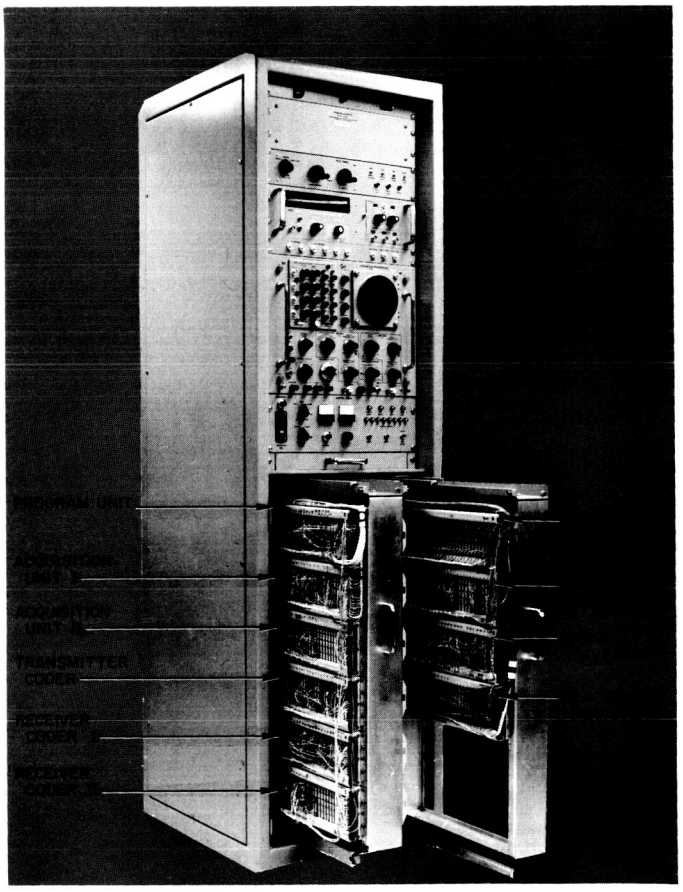


Fig. 33. Mark I ranging subsystem with door removed, showing arrangement of digital assemblies

Fig. 33 shows the ranging subsystem with the front door removed and the left and right T-frames, partly and fully extended, respectively. These frames hold the ten T-Bloc digital assemblies. It will be noted that the possibility of extending the T-frames provides easy access to the module patch wiring on the left and permits removal of modules on the right. The T-Blocs within a frame are interconnected by wires which run vertically along the sides of the frames. The main signal and power wiring harness interconnects the two T-frames and the remainder of the subsystem. It may be noted (Fig. 34) that a power supply, the analog-to-digital con-

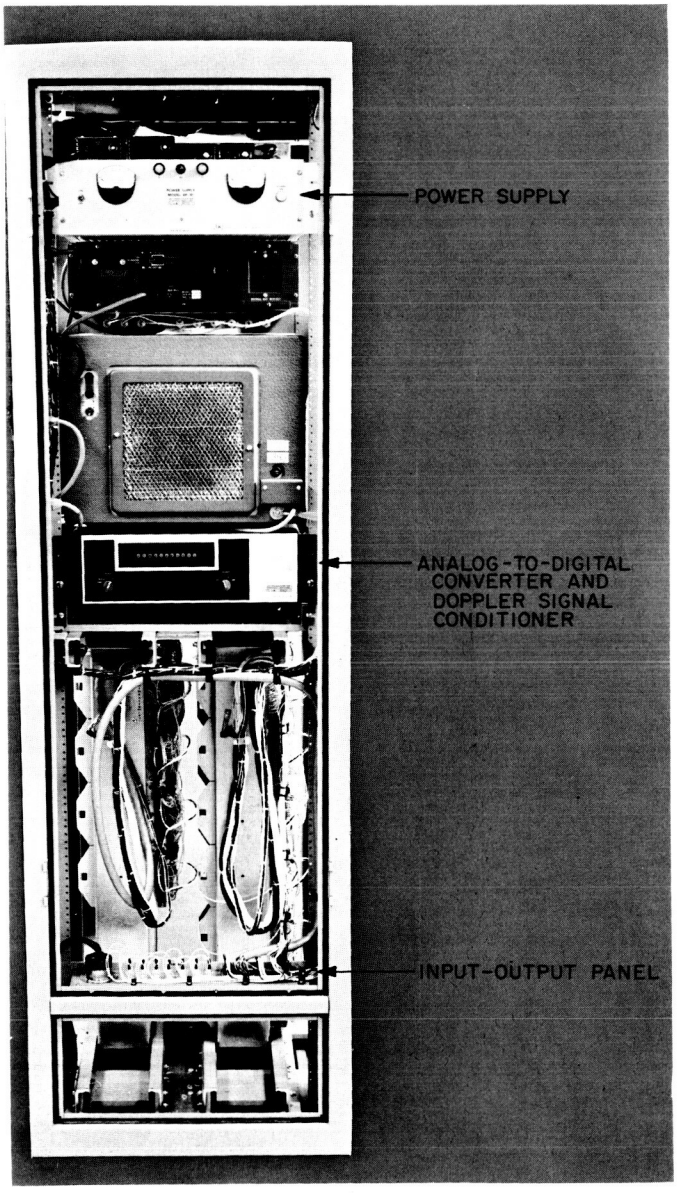


Fig. 34. Mark I ranging subsystem, rear view with door and access panel removed

verter, and the input–output panel are mounted from the rear of the equipment cabinet.

Prototypes of two additional pieces of test equipment have been fabricated. These units, the radio system simulator and the data system simulator, provide essential interface signals for test purposes in the absence of the radio subsystem or the data handling subsystem.

The Serial No. 1 (Pioneer) GSDS subsystem has been installed in the interim S-band control building at Goldstone. It is currently undergoing interface compatibility tests with the S-band radio subsystems and the data handling subsystem. Helicopter ranging and tracking tests will be performed shortly to verify the operational capabilities of the complete S-band tracking station.

H. S-Band Doppler Equations

The doppler equations described in this article are used for extracting S-band doppler from DSIF tracking system observables obtained at either S-band or L- to S-band converted tracking stations. The equations, presented under the operational modes in which they are used, consist of: one-way, two-way, two-way-two-station-coherent, and two-way-two-station-noncoherent. Figs. 35 through 41, which are simplified block diagrams of the modes of operation, contain only those portions of the tracking systems which affect the doppler equations.

To simplify the equations themselves, the doppler shift is written as $f(V(t))$, where f is the frequency being transmitted, or referred to, and $V(t)$ is a function of the velocities of the transmitter, the spacecraft, and the receiver. In the one-way mode, $V(t)$ is approximately equal to $\dot{r}/c$.

1. S-Band Doppler System

a. One-way mode. The one-way mode of operation for the S-band doppler system is shown in Fig. 35; the following definitions apply to it.

$f_{(X\text{-}MIT\ SC)}$ = frequency transmitted by the spacecraft.

$V(t)$ = velocity portion of doppler shift equation; in one-way mode $\approx \dot{r}/c$.

f_{rec} = received frequency at the station = $(f_{(X\text{-}MIT\ SC)})(1 - V(t))$.

$f_{(X\text{-}MIT\ VCO)}$ = frequency of the station transmitter VCO = Kf_R for normal operation in the one-way mode.

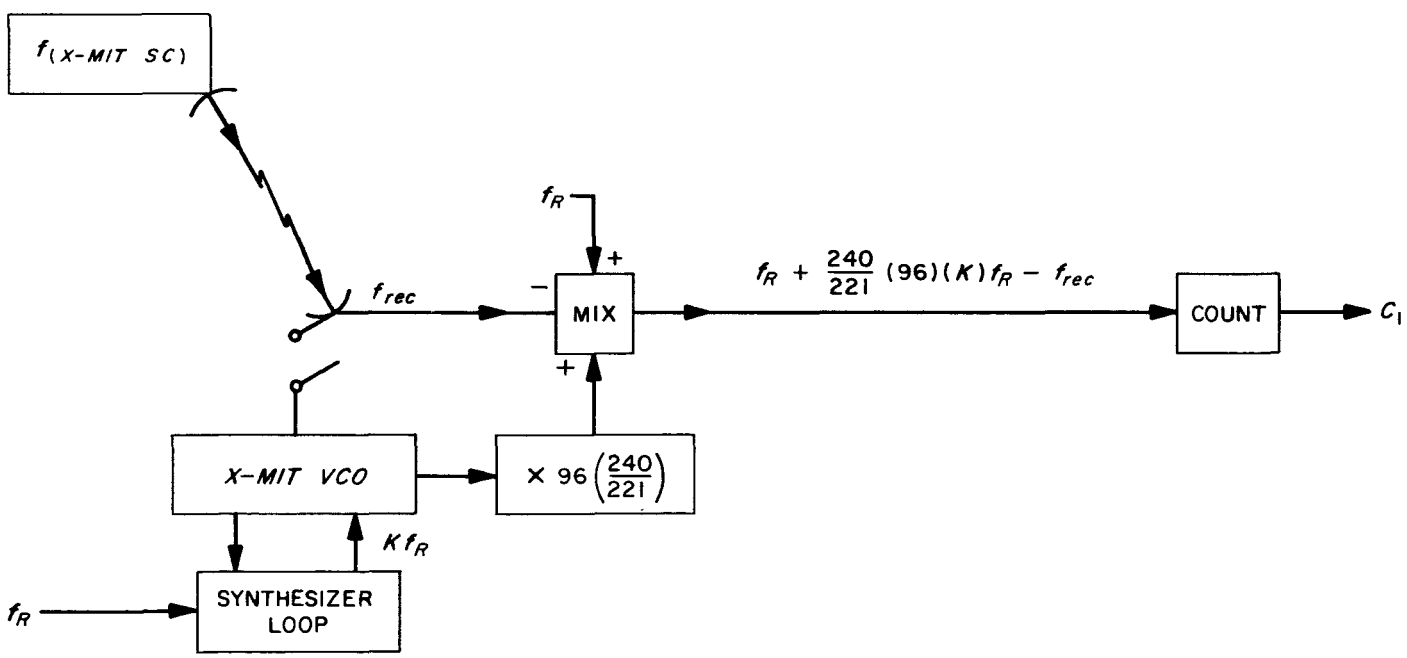


Fig. 35. S-band one-way mode

K = synthesizer multiplier value. K can be set between 21.9472 and 22.0528 in steps of 0.000001. K must be set so that $\left[\left(\frac{240}{221}\right) 96\, Kf_R - f_{rec}\right] < 2 \times 10^5$.

f_R = frequency reference = 1×10^6 cps to one part in 10^{10}, or better.

f_B = doppler bias = 1×10^6 cps to $\approx$ one part in 10^{12}. To indicate where the bias occurs in the equation, it will be circled in the equation, e.g., $\textcircled{10^6}$.

f_D = doppler frequency = $(f_{(X\text{-}MIT\ SC)})\,(V(t)) \approx \dot{r}/c\,(f_{(X\text{-}MIT\ SC)})$.

T_1 = doppler count time.

C_1 = counted number of doppler cycles = $f_D(T_1) \pm 1$. The ± 1 is due to counter roundoff.

The following observables are obtained from doppler equipment at the tracking stations and are encoded by the data handling equipment for transmission to the Space Flight Operations Facility (SFOF) at JPL.

$$C_1 = \left[f_R + \left(\frac{240}{221}\right) 96\, Kf_R - (f_{(X\text{-}MIT\ SC)})\,(1 - V(t)) \right] \frac{10^6 T_1}{f_R} \pm 1$$

thus

$$C_1 = \left[\textcircled{10^6} + \left(\frac{240}{221}\right) 96\,(K)\, 10^6 - (f_{(X\text{-}MIT\ SC)})\,(1 - V(t))\, \frac{10^6}{f_R} \right] T_1 \pm 1.$$

To extract $\dot{r}/c$, which is $\approx V(t)$, from the above equation, an estimate must be made of $f_{(X\text{-}MIT\ SC)}$.

b. Two-way mode. The two-way mode of operation for the S-band doppler system is shown in Fig. 36. The following definitions apply to it.

f_{rec}, $f_{(X\text{-}MIT\ VCO)}$, f_R, f_B, T_1, C_1 = same definitions as used in the one-way mode.

$V(t)$ = velocity term in doppler equation $\approx 2\dot{r}/c$.

$f_{(X\text{-}MIT)}$ = transmitted frequency = $96\,(f_{(X\text{-}MIT\ VCO)})$.

f_D = doppler frequency = $(f_{(X\text{-}MIT)})\,(240/221)\,(V(t)) \approx (f_{(X\text{-}MIT)})\,(240/221)\,(2\dot{r}/c)$.

If the transmitter VCO is locked to the synthesizer, $f_{(X\text{-}MIT\ VCO)} = Kf_R$ and

$$C_1 = \left\{ f_R + \left[\left(\frac{240}{221}\right) 96\, Kf_R\, (V(t)) \right] \right\} \frac{10^6 T_1}{f_R} \pm 1$$

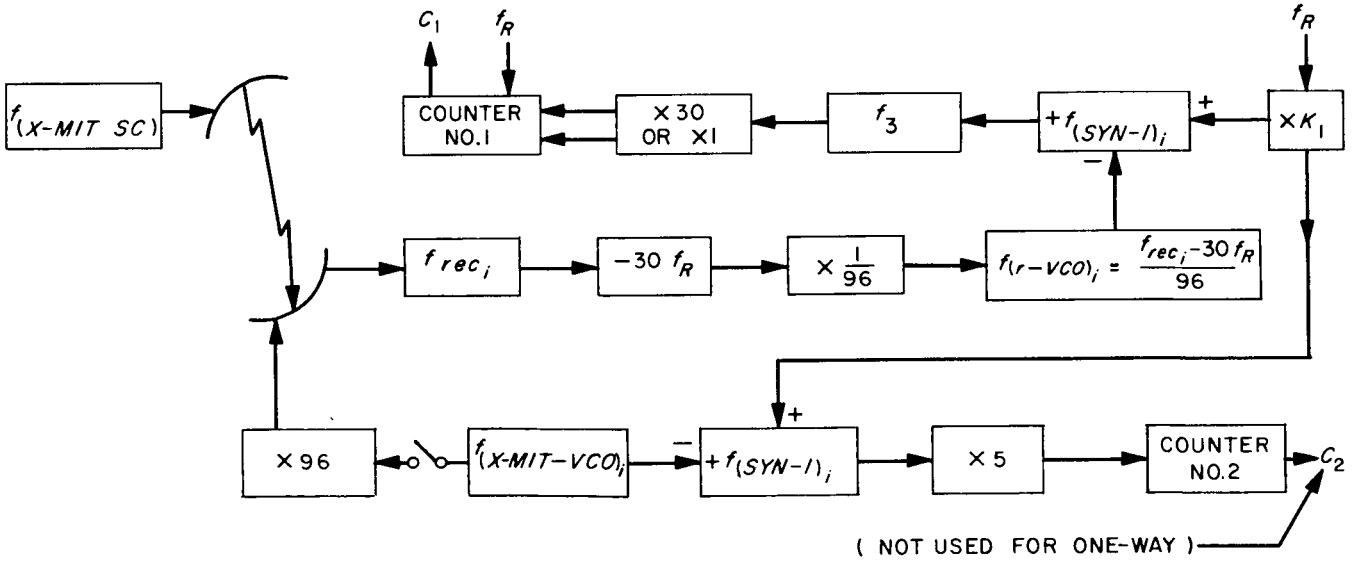


Fig. 36. S-band two-way mode

thus

$$C_1 = \left[\textcircled{10^6} + \frac{240}{221}(96)\, K\, 10^6\, (V(t)) \right] T_1 \pm 1.$$

If the transmitter VCO is not locked to the synthesizer, the frequency of the VCO must be obtained by counting $f_{(X\text{-}MIT\ VCO)}$. Let this count equal C_2, where $3(f_{(X\text{-}MIT\ VCO)})$ is counted for a period of T_2. Thus, $C_2 = 3(f_{(X\text{-}MIT\ VCO)})\, T_2 \pm 1$ and

$$C_1 = \left[\textcircled{10^6} + \frac{240}{221}(96)\left(\frac{C_2 \pm 1}{3T_2}\right)(V(t)) \right] T_1 \pm 1.$$

c. Two-way-two-station-coherent mode. This mode of operation for the S-band doppler system is shown in Fig. 37. The transmitter station can transmit only, or it can operate in the two-way mode. In the latter case, the equations from the two-way mode must be used for data received at the transmitting station. For the receiver station (which receives only) all symbols are the same as those used in two-way station mode except for $V(t)$, f_D, and f_R. The following symbols and definitions apply in the two-way-two-station-coherent mode.

$V(t)_{STA.\ t \to SC}$ = velocity term of doppler shift
$\approx \dot{r}_{STA.\ t \to SC}/c$
where $\dot{r}_{STA.\ t \to SC}$ is the range rate on the transmitter-to-spacecraft link.

$V(t)_{SC \to STA.\ rec}$ = velocity term of doppler shift
$\approx \dot{r}_{SC \to STA.\ rec}/c$
where $\dot{r}_{SC \to STA.\ rec}$ is the range rate on the spacecraft-to-receiver link.

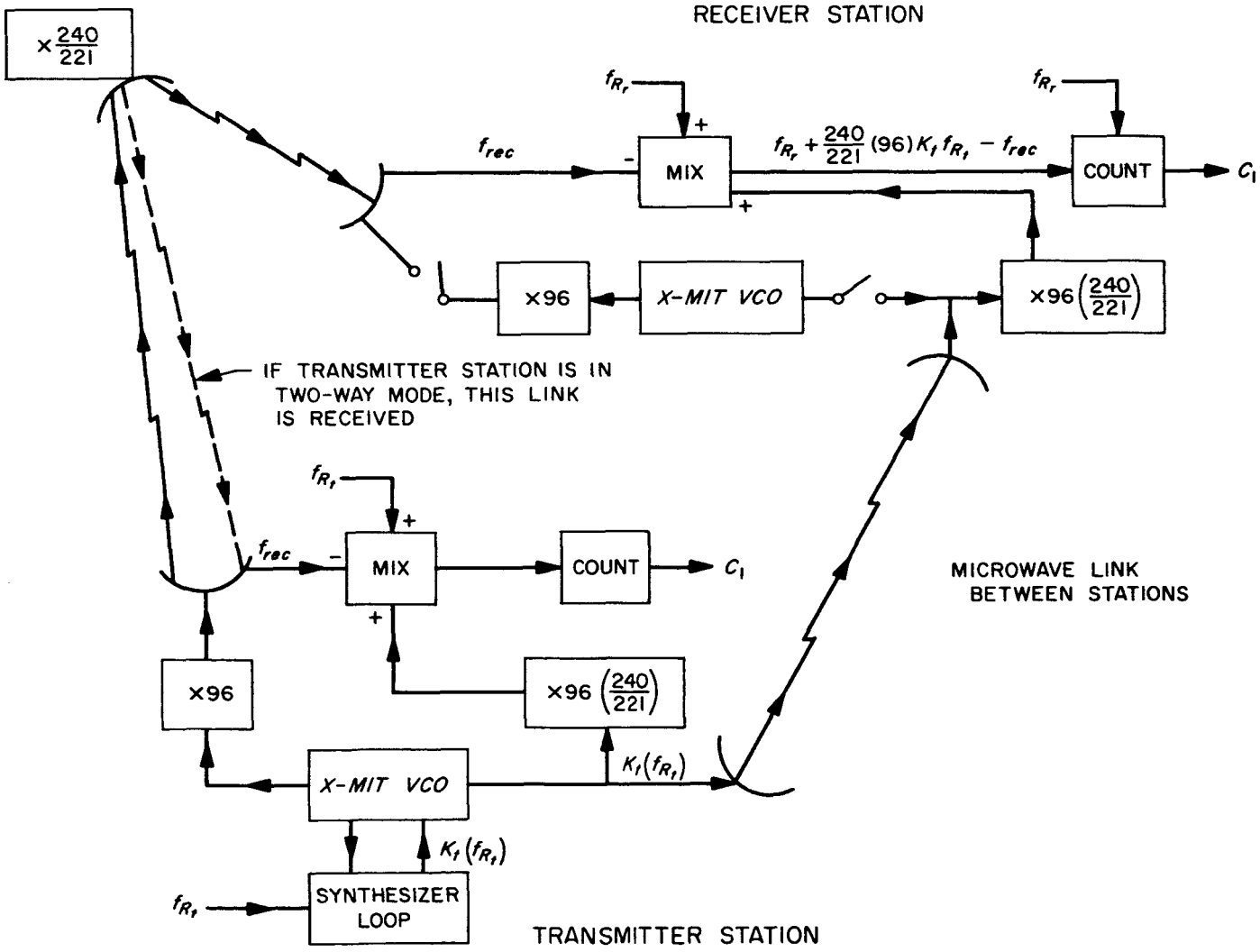


Fig. 37. S-band two-way-two-station-coherent mode

$$V(t) \approx V(t)_{STA.\ t \to SC} + V(t)_{SC \to STA.\ rec}$$

f_{R_t} = frequency of frequency reference of transmitter station.

f_{R_r} = frequency of frequency reference of receiver station.

$$f_D = \left[\left(\frac{240}{221}\right) 96\, K_t f_{R_t}\right]\left[1 - (1 - V(t)_{STA.\ t \to SC})(1 - V(t)_{SC \to STA.\ rec})\right]$$

Thus, when the transmitter station's transmitter VCO is locked to the synthesizer and the output is $K_t f_{R_t}$, $C_1 = [\ (10^6) + (240/221)\, 96\, K_t f_{r_t}\, (10^6/f_{R_r})\, V(t)]\, T_1 \pm 1$.

When the transmitter station's transmitter is not locked to the synthesizer, solve the above equation by replacing $K_t f_{R_t}$ with $(C_2 \pm 1)/3T_2$, where $C_2 = 3\,(f_{(X\text{-}MIT\ VCO)})\, T_2 \pm 1$ and is measured at the transmitter station.

d. Two-way-two-station-noncoherent mode. This mode of operation for the S-band doppler system is shown in Fig. 38. When the transmitter station is in two-way lock, the same equations apply for data received at the trans-

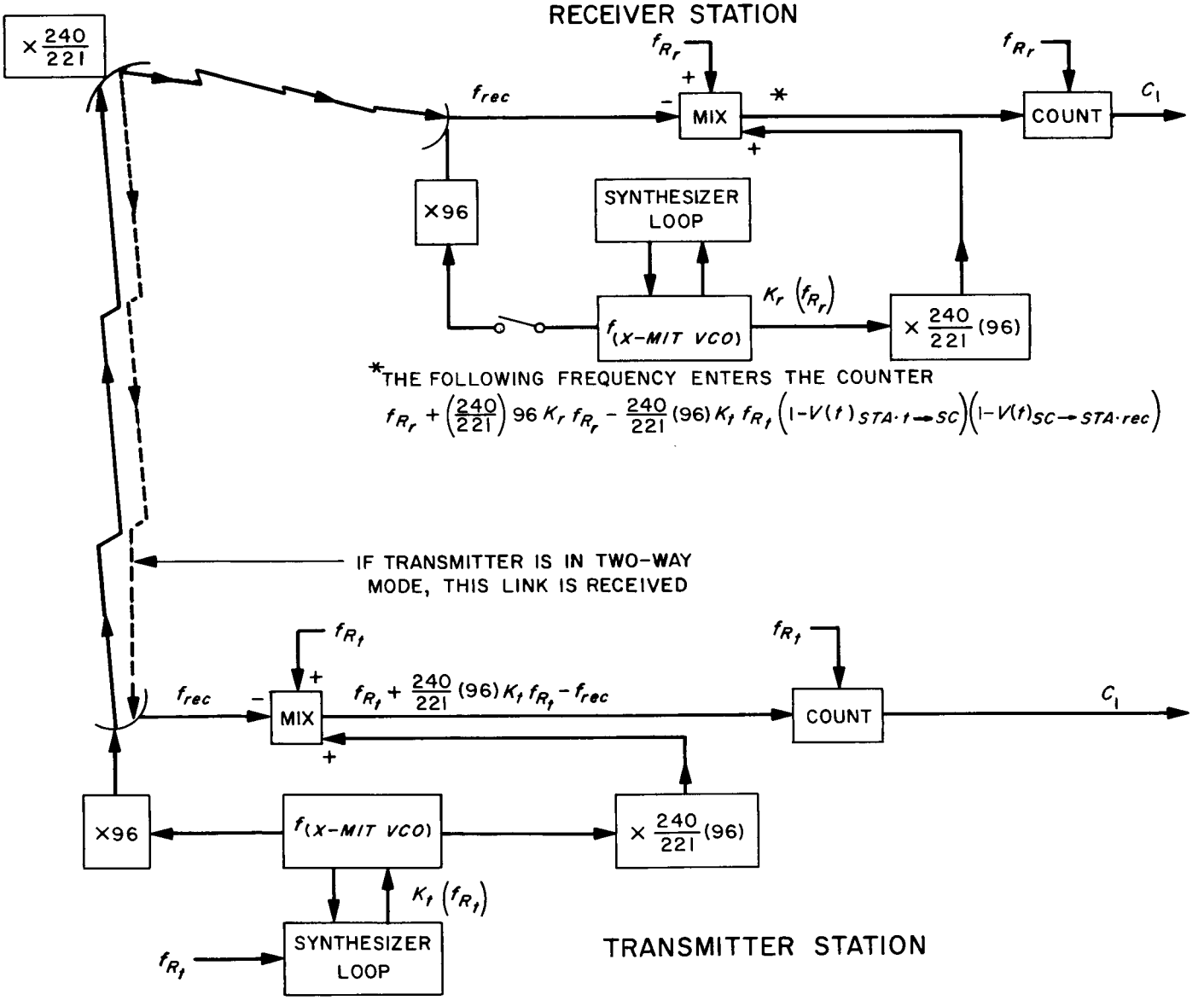


Fig. 38. S-band two-way-two-station-noncoherent mode

mitting station as those used in the two-way mode. For the receiver station, all symbols are the same as those used in the two-way-two-station-coherent mode. For this mode then,

$$C_1 = \left\{ 10^6 + \left[\left(\frac{240}{221}\right) 96 \frac{K_r f_{R_r}}{f_{R_r}} 10^6 - \left(\frac{240}{221}\right) 96 \frac{K_t}{f_{R_r}} f_{R_t} \left(1 - V(t)_{STA.\,t \to SC}\right) \times \left(1 - V(t)_{SC \to STA.\,rec}\right) 10^6 \right] \right\} T_1 \pm 1.$$

It must be noted that K_r is not necessarily equal to K_t, nor is f_{R_t} necessarily equal to f_{R_r}. K_r, however, must be set so that the doppler bandwidth is less than 2×10^5 cps. If the transmitter or receiver station has not locked its transmitter VCO to the synthesizer, replace $K_r f_{R_r}$ with $(C_2 \pm 1)/3T_2$ from the receiver station and $K_t f_{R_t}$ with $(C_2 \pm 1)/3T_2$ from the transmitter station to solve the above equation.

2. L- to S-Band Conversion System

For L-band operations, standard L-band equations will apply. The symbols and definitions used in the L- to S-band equations are given below.

$C_1 = T_1 f_1$ = output of counter No. 1.

f_1 = 30.0 (f_3) for precision operation, which is the standard case, or 1.0 (f_3) for non-precision operation.

$C_2 = 1 f_2$ = output of counter No. 2.

$f_2 = 5\,[f_{(SYN-1)_i} - f_{(X\text{-}MIT\ VCO)_i}]$

$f_3 = (f_{(SYN-1)}) - (f_{r_i} - 30 f_R/96)$ = detector output.

$f_{(X\text{-}MIT\ VCO)_i}$ = frequency of transmitter VCO at station (i).

$f_{t_i} = 96\,(f_{(X\text{-}MIT\ VCO)_i})$ = frequency transmitted by station (i).

$f_{(X\text{-}MIT\ SC)}$ = frequency of the transponder in auxiliary drive mode (one-way mode).

M_{SC} = 240/221 = spacecraft transponder frequency multiplier.

f_{rec_i} = received frequency at station (i).

$f_{(r\ VCO)_i}$ = frequency of the receiver VCO at station (i).

$f_{(SYN\ j)_i}$ = frequency of frequency synthesizer (j) at station (i). The frequency settings of the frequency synthesizers will be included in the station reports. $f_{(SYN\ j)} = (K_j)\,(f_{R_i})$.

f_{R_i} = frequency reference for station (i) = 1 Mc nominal.

f_D = doppler frequency = $(f_{t_i})\,((V(t))\,(240/221)$.

All units of frequency are in megacycles.

a. One-way mode. The one-way mode of operation for the L- to S-band doppler system is shown in Fig. 39.

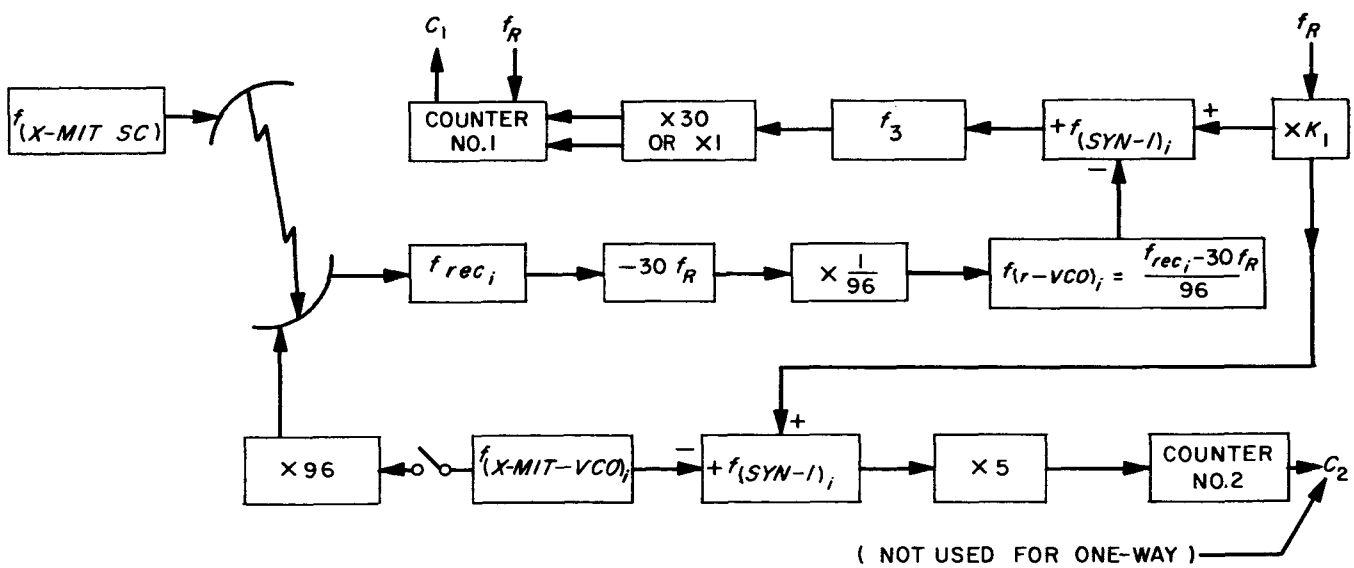


Fig. 39. L- to S-band one-way mode

The following equations are applicable to the one-way mode.

$$f_{r_i} = (f_{(X\text{-}MIT\,SC)})\,(1 - V(t)_{SC\to i})$$

$$f_{(r\,VCO)_i} = \frac{f_{rec_i} - 30 f_R}{96}$$

$$f_1 = 30 f_3 = 30\left\{ f_{(SYN-1)} + \frac{30 f_R}{96} - \frac{(f_{(X\text{-}MIT\,SC)})\,(1 - V(t)_{SC\to i})}{96}\right\}$$

If we assume $V(t)_{SC\to i} \approx \dot{r}/c$

$$C_1 \approx \left[30 K_1 f_R + \frac{900 f_R}{96} - \frac{30}{96} f_{(X\text{-}MIT\,SC)}\left(1 - \frac{\dot{r}}{c}\right)\right]\frac{10^6 T_1}{f_R}$$

where T_1 is the count time.

To extract f_D, an estimate of $f_{(X\text{-}MIT\,SC)}$ must be made.

b. Two-way mode. Fig. 40 shows the two-way mode of operation for the L- to S-band doppler system. The following equations are applicable to the two-way mode. When the synthesizer is used, $f_{(X\text{-}MIT\,VCO)_i} = K_2 f_R$. Otherwise, $f_{(X\text{-}MIT\,VCO)_i} \approx f_{(SYN-1)_i} - C_2/5T_2$, where T_2 is equal to 1 sec.

$$f_{rec_i} = 96 f_{(X\text{-}MIT\,VCO)_i}\left(\frac{240}{221}\right)(1 - V(t))$$

$$C_1 = \left[30 f_{(SYN-1)} + \frac{900 f_R}{96} - 30\left(\frac{240}{221}\right) f_{(X\text{-}MIT\,VCO)_i}\,(1 - V(t))\right]\frac{10^6 T_1}{f_R}.$$

If we assume $V(t) \approx 2(\dot{r}/c)$,

$$C_1 = \left[30 K_1 f_R + \frac{900 f_R}{96} - 30\left(\frac{240}{221}\right) f_{(X\text{-}MIT\,VCO)_i}\left(1 - 2\frac{\dot{r}}{c}\right)\right]\frac{10^6 T_1}{f_R}$$

$$C_2 = 5\,(K_1 f_R - f_{(X\text{-}MIT\,VCO)_i}) \pm 1 \text{ count.}$$

When the transmitter VCO is locked to the synthesizer, $f_{(X\text{-}MIT\,VCO)_i} = K_2 f_R$. When the transmitter VCO ± 1 is not locked to the synthesizer, $f_{(X\text{-}MIT\,VCO)_i} = K_1 f_R - C_2/5$.

In this mode, $f_{(X\text{-}MIT\,VCO)_i}$ can only be assumed to be correct to one part in 10^8. If a $f_{(X\text{-}MIT\,VCO)_i}$ which is correct to one part in 10^8 is used to compute C_1, the residuals formed from $|C_{1(DATA)} - C_{1(COMPUTED)}|$ will be on the order of $+6.5 T_1 + 1/T_1$. This is equivalent to a 21-cps residual in the doppler frequency, i.e.,

$$f_D = 2295 \times 10^6\,(2r/c) \pm 21 \text{ cps.}$$

When the transmitter VCO is locked to the frequency synthesizer, the residual formed from

$$|C_{1(DATA)} - C_{1(COMPUTED)}|$$

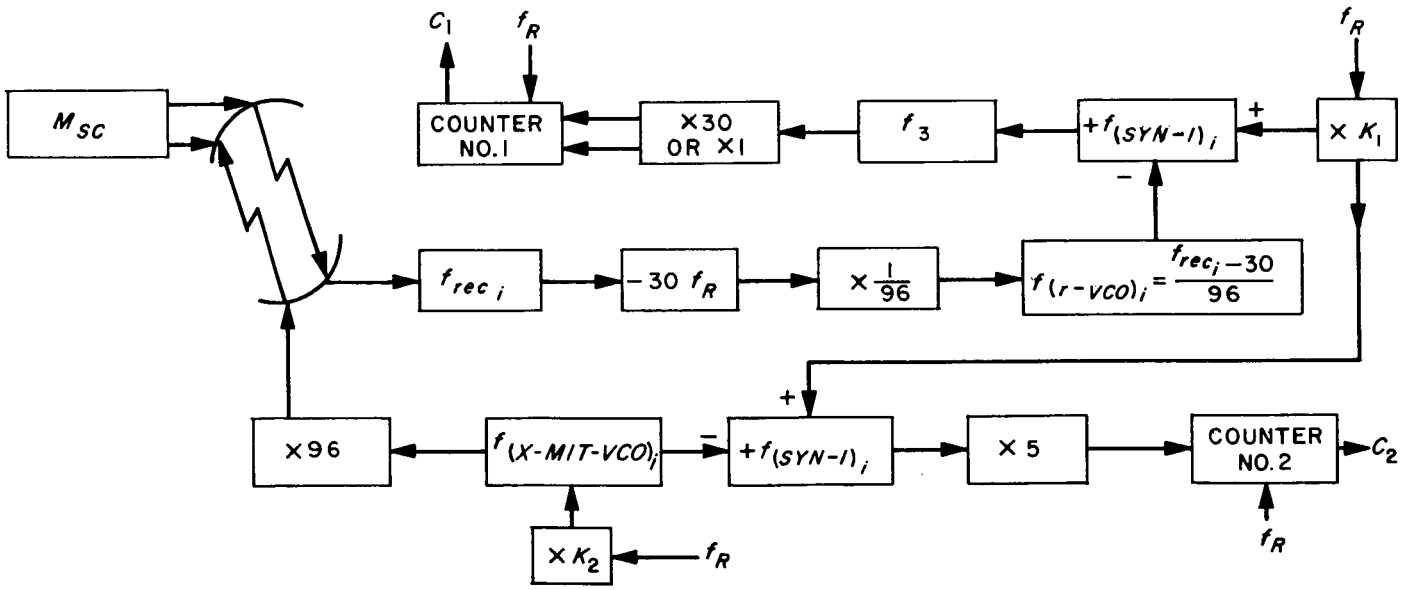


Fig. 40. L- to S-band two-way mode

will be on the order of $+1/T_1$ for $1 \leq T_1 < 100$ sec.

c. Two-way-two-station-coherent mode. Although this mode is used in the S-band system, it does not exist in the L- to S-band conversion system.

d. Two-way-two-station-noncoherent mode. This mode of operation for the L- to S-band doppler system is shown in Fig. 41. The following equations are applicable to this mode.

Let f_{R_t} equal the reference frequency of the transmitter station and f_{R_r} equal the reference frequency of the receiver station. If either an S- or L- to S-band station is transmitting, f_{t_t} is equal to $96\,K_{2_t} f_{R_t}$ if the transmitter station's VCO is locked to the synthesizer.

$$f_{r_r} = 96\,(K_{2_t} f_{R_t})(1 + V(t)_{STA.\,t \to SC}) \times \frac{240}{221}\left(1 + V(t)_{SC \to STA.\,rec}\right)$$

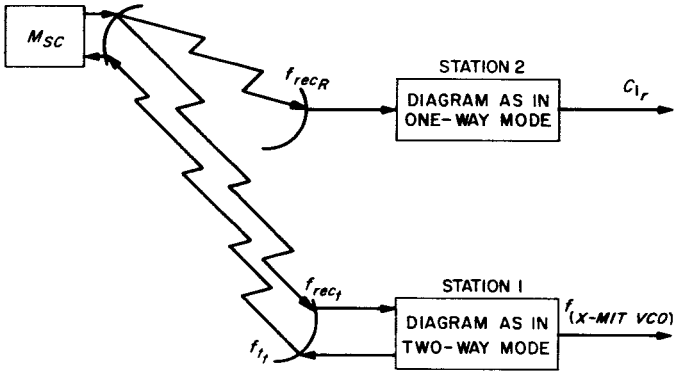


Fig. 41. L- to S-band two-way-two-station-noncoherent mode

$$C_{1_r} = \left(30\,K_{1_r} f_{R_r} + \frac{900}{96} f_{R_r} - \frac{30 f_{r_r}}{96}\right)\frac{10^6\,T_1}{f_{R_t}}.$$

If we assume $V(t)_{STA.\,t \to SC}$ on the up-leg is equal to $-\dot{r}_{t \to SC}/c$, and $V(t)_{SC \to STA.\,rec}$ on the down-leg is equal to $-\dot{r}_{SC \to STA.\,rec}/c$, then when we compute C_{1_r}, we find:

$$C_{1_r} = \left\{30\,K_{1_r} f_{R_r} + \frac{900}{96} f_{R_r} - 30\,(K_{2_t} f_{R_t}) \times \left(1 - \frac{\dot{r}_{STA.\,t \to SC}}{c}\right)\left(1 - \frac{\dot{r}_{SC \to STA.\,rec}}{c}\right)\left(\frac{240}{221}\right)\right\}\frac{10^6\,T_1}{f_{R_r}}.$$

3. Reference Frequency Stability at L- to S-Band Stations

The reference frequency f_R is known at the L- to S-band stations to be one part in 10^8. The stability of f_R is three parts in 10^{11} over periods ranging from 1 sec to 1 hr. The 24-hr stability is three parts in 10^{10}.

If VLF receivers and rubidium standards are available at the L-S sites, the reference frequency will have the same stability, and the ability to measure absolute frequency will be the same as at S-band sites. At S-band sites, f_R is known to an accuracy of one part in 10^{10}, and has a stability of two parts in 10^{11} over periods of 1 sec to 20 min. The long term 1-yr stability is even better than the above mentioned figures.

References

1. "Project Engineering," *SPS 37-26*, Vol. III, p. 12, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.
2. "Cassegrain System, 960 Mc," *SPS 37-14*, Vol. I, pp. 99–107, Jet Propulsion Laboratory, Pasadena, California, April 1, 1962.
3. "System Integration and Engineering," *SPS 37-26*, Vol. III, p. 16, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.
4. "Acquisition Aid for DSIF," *SPS 37-24*, Vol. III, pp. 79–81, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

References (Cont'd)

5. "Acquisition Aid for DSIF," *SPS 37-25,* Vol. III, p. 53, Jet Propulsion Laboratory, Pasadena, California, January 31, 1964.

6. "TWM for DSIF," *SPS 37-25,* Vol. III, pp. 51—53, Jet Propulsion Laboratory, Pasadena, California, January 31, 1964.

7. "Equipment," *SPS 37-24,* Vol. III, pp. 5–8, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

8. "Receiver Modifications," *SPS 37-25,* Vol. III, pp. 5–6, Jet Propulsion Laboratory, Pasadena, California, January 31, 1964.

9. "Mark I Ranging Subsystem," *SPS 37-20,* Vol. III, pp. 12–15, Jet Propulsion Laboratory, Pasadena, California, March 31, 1963.

10. "Helicopter Tests Simulating Lunar Ranging," *SPS 37-18,* Vol. III, pp. 52–54, Jet Propulsion Laboratory, Pasadena, California, November 30, 1962.

11. "Test Panel," *SPS 37-24,* Vol. III, p. 11, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

12. "Control Panel," *SPS 37-24,* Vol. III, pp. 9–10, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

III. Space Flight Operations Facility

A. Mission Status Board

The Space Flight Operations Facility (SFOF) has been described in previous issues of *SPS*, Vol. VI. The mission status board, located in the operations area of the SFOF, is capable of displaying summary information for two simultaneous missions. Contained in the mission status board are three unique display devices: the Eidophor television projector, the mission events display projector, and various types of relatively simple semiautomatic displays. These are described here.

1. Eidophor Television Projector

The Eidophor television projector is shown in Fig. 1. The bright picture projected by the Eidophor derives the light not from the conventional projection cathode ray tube, but from a powerful Xenon arc lamp (1.6 kw). The projected picture is of such size and brightness that it is comparable to those produced on a cinema screen. Light from the arc lamp is thrown via mirrors onto a thin film of oil in the Eidophor on which is impressed an electrostatic image of the picture to be projected. This electrostatic image causes local deformations on the oil film which, being strongly illuminated, is capable of being projected by an optical system onto a rear projection screen. This control layer system was given the name Eidophor, which means "image bearer" in Greek.

The principle of the control layer system is illustrated in the schematic drawing shown in Fig. 2. Fig. 3 is a perspective drawing which further illustrates the principle involved. These two illustrations are essentially identical in construction except that, for simplicity, the indirect light path has been omitted in Fig. 2. The reference numbers apply to both.

Light Source 2, a Xenon arc lamp which uniformly illuminates Picture Window 6, is imaged by means of an efficient dual light path lens system (Fig. 3) on Mirror Bars 9a, b, and c. For convenience, only three of the six bars comprised in the Eidophor projector are shown in the two illustrations.

The purpose of Converging Lens 7 and Field Lens 8 is to image Picture Window 6 onto Spherical Mirror 10

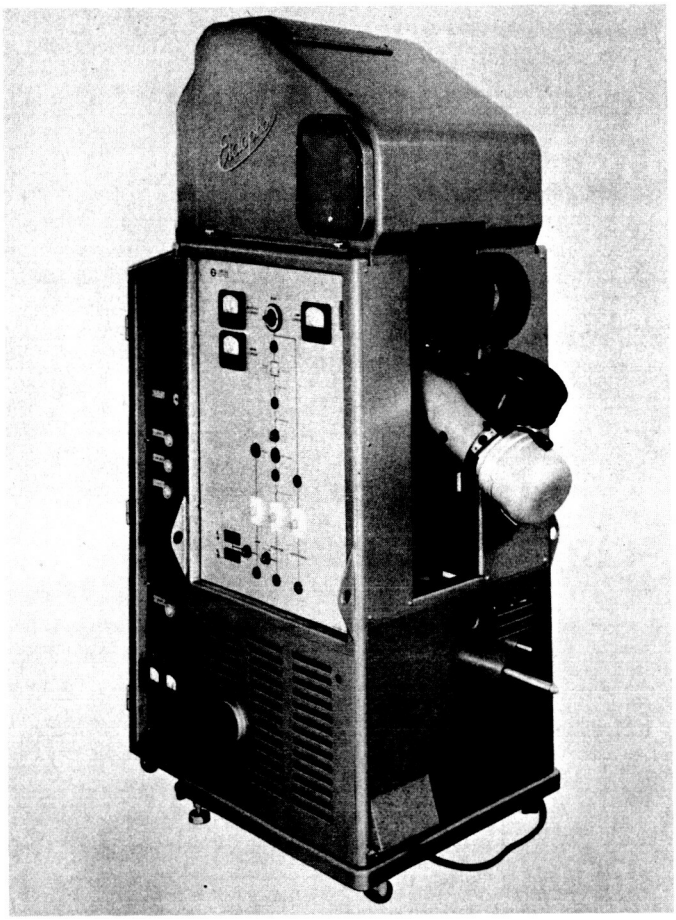


Fig. 1. Eidophor television projector

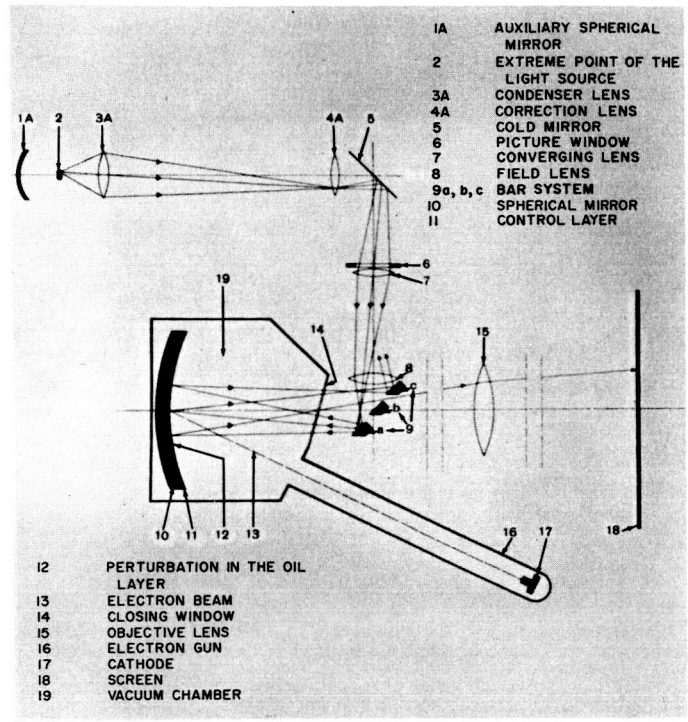


Fig. 2. Eidophor control layer principle, schematic

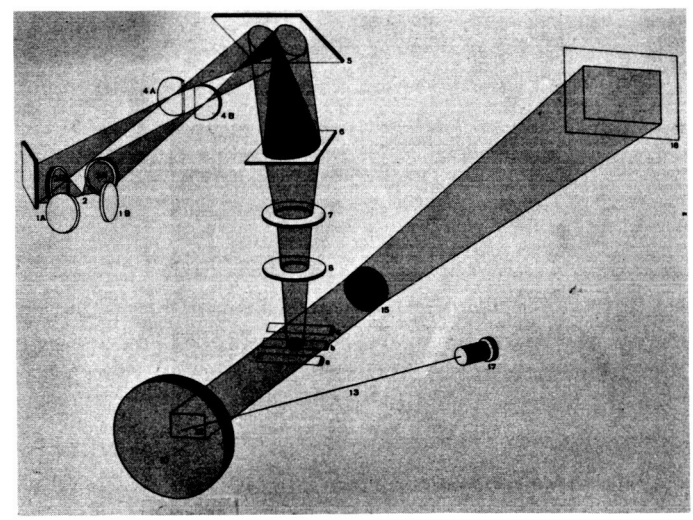


Fig. 3. Perspective of Eidophor control layer system

via Bar System 9. Because the center of Bar System 9 coincides with the center of the illuminated section of the Spherical Mirror 10, the bar system is imaged in itself. This means that light coming from any point in the opening of Picture Window 6 and falling onto a mirror bar (e.g., 9a) and from there onto Spherical Mirror 10, is reflected by this mirror toward a symmetrically situated mirror bar (9c) from where it is returned to the symmetrical point in Light 2. The reflecting sides of the bar system are not arranged in a plane but rather in the position of slats in a Venetian blind. The purpose of this arrangement is to ensure that all light thrown from the source toward the bar system, viewed from the direction of illumination, appears as a continuous plane without slots, whereas, seen from the mirror side, the apertures permitting the passage of the light deflected by the rippled oil layer are visible.

The Electron Gun 16 consists of a cathode, the electrostatic modulation lens, the focusing coil, and the deflection yoke.

The electron gun, the whole mirror cassette, and the control layer oil pump must be continuously evacuated during operation. To produce and to maintain the required high vacuum of less than 10^{-4} mm Hg, the projector uses a mechanical forepump in conjunction with a high-vacuum oil diffusion pump.

The video sweep and power supply chassis is of conventional electronic design.

2. Mission Events Display Projector

This display projector, procured from Western Electrosystems, Inc., per JPL specifications, will show a continuous real-time relationship between event information and current time in each of the selectable time scales. The display employs dual independent projectors as shown in Fig. 4. The top projector, called the static unit, has a 7.6- × 10-in. field producing a bright 66.5- × 88-in. image of the mission event data and symbology. The lower projector, referred to as the cursor unit, is also based upon the same aperture, and generates selectable time cursor sweeps at rates of 1 in./min, 1 in./hr and 1 in./day. The remaining volume contains the power supply and cooling fans.

The image/object geometries are similar to those of conventional high quality opaque and transparency projectors. The composite image is synthesized or optically

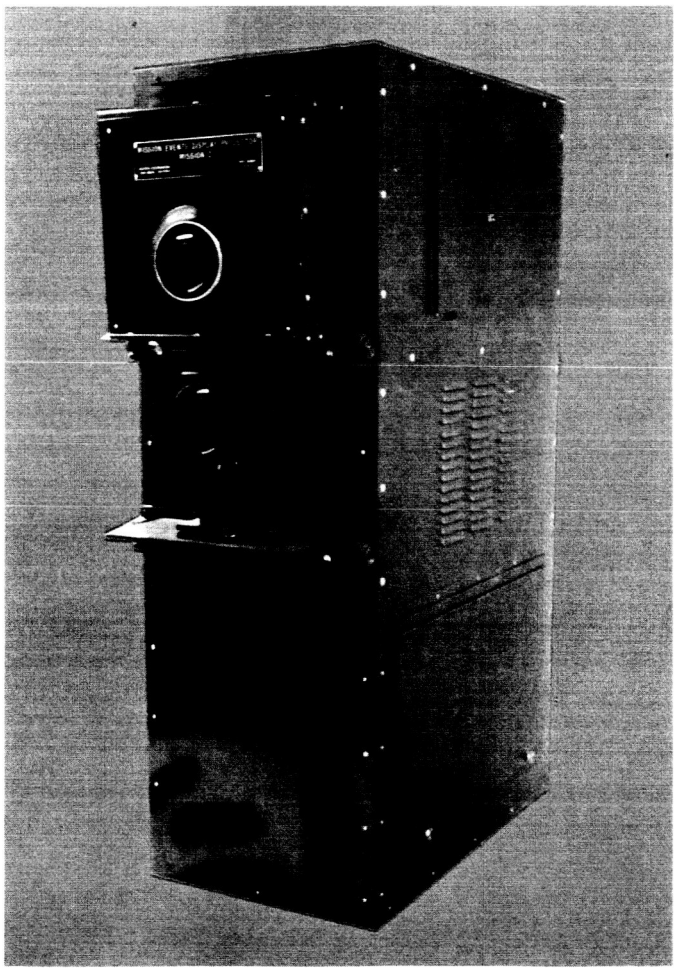


Fig. 4. Mission events display dual independent projectors

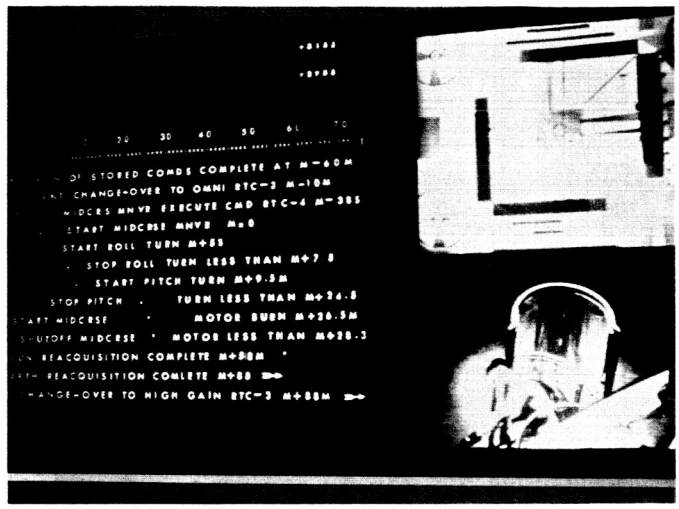


Fig. 5. Rear projection screen

mixed by back illumination of a high efficiency, diffused, rear projection transmissive screen. The rear projection screen (Fig. 5) uses elasticized cloth for attachment to a wood frame and can be removed from the steel mission status board main frame for cleaning and maintenance. Symbology and alphanumeric characters are projected as high brilliance images on a black background; the cursor image appears as a bright vertical line. Full use can be made of polychromatic high contrast display techniques in the event that the operating group desires to employ such techniques in order to enhance physiological effectiveness. It is anticipated, however, that high contrast white on black, or negative projection, will be routinely employed for ease in updating and remote TV monitoring. The cursor projector will slew the cursor image at a uniform timing rate corresponding to the selected mission event period. The remote control box (Fig. 6), located on the information coordinator's table, controls

Fig. 6. Remote control box

rate selection, cursor positioning rapid slew, cursor intensity, and on-off switches. The electrical system provides all manual control, indication, and safety interlock features.

The operational readiness of the system is enhanced by the inclusion of a flexible display platen (Fig. 7), permitting the rapid updating of the specific data to reflect changes in mission content and/or sequences. The updating can be accomplished by replacing the entire platen or by replacing one or more of the 16-line message carriers, or by replacing the individual letters or symbols within a particular line message carrier.

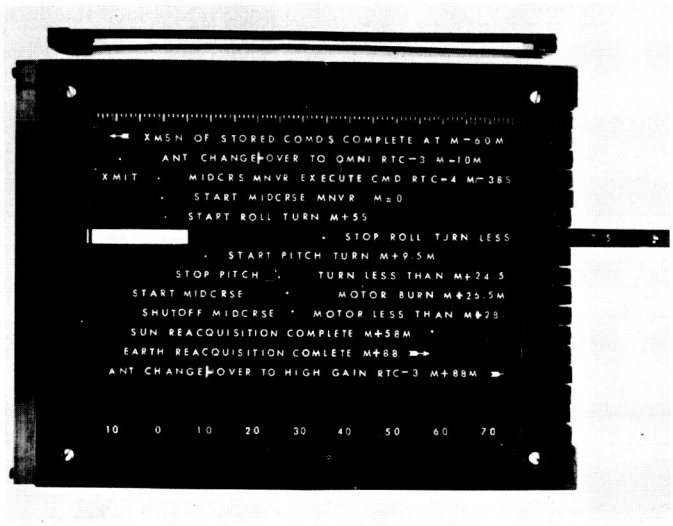


Fig. 7. Flexible display platen

The reliability of the projector and controls is maximized by: (1) selection of rugged piece parts, (2) temperature derating of electromechanical devices, (3) holding low rotational speeds on drive motors, (4) minimizing actuation on relays and contactors, and (5) derating source lights and other heat dissipative elements in an equivalent manner to semiconductors.

3. Semiautomatic Displays

Two typical semiautomatic display modules are shown in Fig. 8; each displays a different type of operational summary and semidetailed technical information peculiar to a particular mission. These modules, approximately 7 ft high, 3 ft wide, and 1 ft deep, are of light construction, aluminum angle-framing and hard-faced masonite. They can be removed from the mission status board steel frame with ease. The names of parameters, items, sensors, and their units or dimensions will be prepared on name-

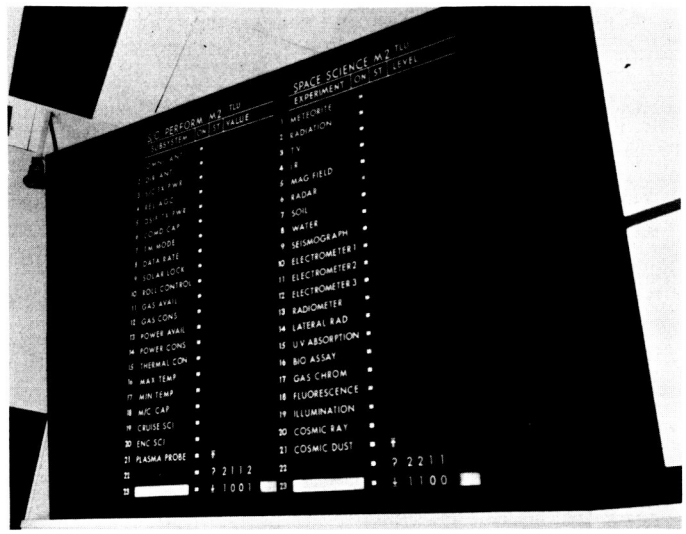


Fig. 8. Semiautomatic display modules

plates prior to or during a mission. A few nameplates have been removed for illustration in Fig. 8. The nameplates are changed from the projection booth behind the mission status board. Pressure sensitive letters or symbols are applied to the nameplates fairly rapidly. The minimum letter size is 1¼ in., which can be viewed at maximum distance of 40 ft. There are sufficient spare nameplates so that light holes, as shown in Fig. 8, should not be viewed for more than a few seconds until a replacement nameplate is snapped into that position.

The module is controlled remotely by a display control assembly (Fig. 9) located in the appropriate technical area director's console. The display control assembly

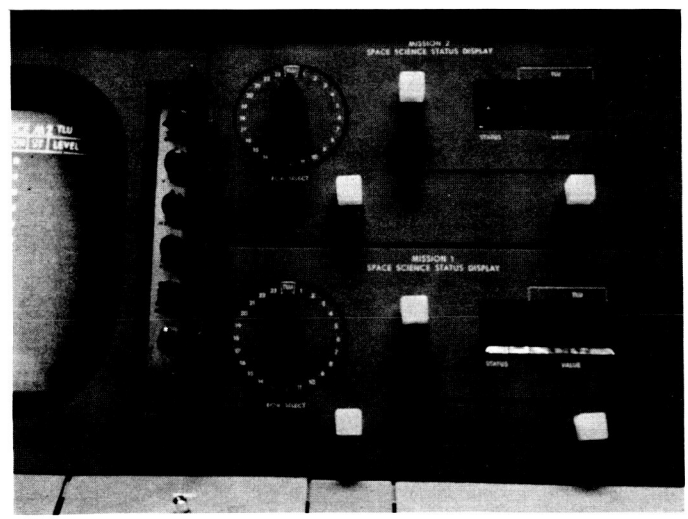


Fig. 9. Display control assembly

controls only the numeric and symbol indicators (digital data indicators) and the condition lights on the module. The control assembly is capable of entering the variable information in any row, one row at a time. The maximum update time for a row of digital data indicators is 3 sec. The controls are fairly straightforward and easily understood after one orientation.

4. Video Lighting Problems

A problem arises in lighting the mission status board in the SFOF for closed circuit TV viewing. The source of the difficulty is the divergence between the acceptable ambient light thresholds for the human eye and for the vidicon camera. The ambient level and characteristic of the SFOF operations area illumination are optimum for the visual tasks involved considering the luminance of rear projected and front lighted displays used. Both the eye and the vidicon require a low contrast ratio between rear projection and front lighted displays which occur in the same view field. The absolute levels required, however, are not the same. It has been necessary to add special lighting for front lighted portions of the mission status board which exhibit different luminance levels to the eye and to the vidicon camera. This was accomplished by making use of another difference between the camera and the eye, i.e., color sensitivity. A light blue filter over the special lights drops the photopic luminance while maintaining the scotopic or camera sensitive luminance value required. The positioning of this special lighting (in the form of framing spotlights) meets additional problems caused by a difference between eyes and cameras, and a difference in viewing position at either the eye or the camera. Located at the opposite end of a spotlight ray reflected from a display character, either an eye or camera "sees" a "hot spot" or specular reflection which totally obliterates the character distinction as well as introduces glare or flare intolerable both to human and camera systems. The solution to this problem of linear programming is most easily found by two-plane ray tracing and requires some trade-offs in locating optimum viewing positions.

B. SFOF Operations

The SFOF operations activities were concentrated into four major areas: internal testing of the SFOF systems, orientation of personnel with respect to use of the SFOF systems, scheduling the SFOF, and establishing standard operating procedures.

1. SFOF Internal Tests

Relatively mission-independent and facility-oriented tests were conducted to ensure that the SFOF could fulfill its objectives as defined in the SFOF System Specifications.

The objectives of the initial SFOF internal tests were:

(1) Verify that the equipments installed in the SFOF, as a part of the initial development of the SFOF, were operable.

(2) Verify that the capabilities of the initial configuration of the SFOF fulfilled those criteria established in the SFOF System Specifications.

(3) Exercise the mission-independent personnel of the SFOF in the operation of these equipments and verify that personnel and equipments were ready to support mission-dependent operations.

Personnel support for these tests came from the data processing system, communications system, display system, *Mariner C* flight operations, and SFOF operations groups.

The concept and procedures for testing were:

(1) The basic concept was to exercise the equipments and personnel to determine whether equipment capability met the SFOF System Specifications, and to evaluate the quality and acceptability of the performance of the subsystems. Specific standards were established for each test.

(2) Testing consisted of equipment operation by the SFOF mission-independent personnel with SFOF operations group personnel evaluating the operational readiness of equipments and personnel. The testing proceeded logically from demonstrations of equipment subsystems, as they were installed and available, to the testing of groups of equipments in SFOF user areas. The testing of certain groups of equipments was combined with mission-dependent testing in order to assure that a sufficient number of personnel were available and that the testing was accomplished under operational conditions.

Test results were published periodically. Several tests had to be delayed due to late delivery of equipment,

others proved equipment design marginal and slight rework was required before they could be completed. In general, all test results met specifications.

2. Orientation of Personnel

The purpose of the orientation program was:

(1) Familiarize personnel with the operational capabilities and limitations of the SFOF systems.

(2) Acquaint personnel with the different areas of the SFOF.

(3) Provide personnel with practice in operating equipment at console stations and support positions.

The first orientation was limited to mission-independent and selected mission-dependent personnel. The latter were from the *Mariner C* flight operations group, assigned to assist the SFOF operations group with the internal tests. Subsequent orientations were presented to the *Ranger* and *Mariner C* mission-dependent personnel.

Two types of orientation were presented. The first was that in which the personnel were expected to operate equipment, such as communications and TV equipment mounted in operations consoles. The second type of orientation was that in which equipment such as data processing was demonstrated only, being operated by highly qualified and specialized personnel.

Instructors for the orientation program consisted primarily of personnel from those areas responsible for the development or operation of the equipments.

3. Scheduling

Three SFOF schedules are prepared and maintained by the operations group—a 10-day, an 18-mo, and a 5-yr schedule.

a. 10-day schedule. Each Thursday, the various projects present their detailed requirements for SFOF support for a 10-day period, beginning on the following Saturday. This is accomplished by means of a standardized form which requires the requestor to specify date, time, areas, and equipment necessary to support a project. Conflicting requirements are resolved at this meeting and results are then approved by the SFOF operations manager and published as the SFOF 10-day schedule.

b. 18-mo schedule. Shortly before the first of each month, SFOF project engineers furnish information to maintain an up-to-date 18-mo schedule which allows planning necessary to support the various projects. This schedule is much less detailed than the 10-day schedule.

c. 5-yr schedule. A schedule for a 5-yr period is maintained and used for the purpose of funding and design. This is broad in scope and general in nature.

4. Standard Operating Procedures

A standard format and numbering system for SFOF standard operating procedures (SOP's) was established. These SOP's are posted in loose-leaf notebooks, strategically located at operating positions in the SFOF, and maintained by the operations group. SOP's are approved by a system engineer, space flight operations director, or the operations manager before issue.

C. On-Site Data Processing System

Preliminary design of the Deep Space Network (DSN) on-site data processing system was completed during this reporting period. The purpose of the system is to provide standardized general purpose digital computing facilities at the deep space stations in order to process spacecraft telemetry data, spacecraft command data, and station instrumentation data.

A block diagram of the on-site data processing system is shown in Fig. 10. The system contains two virtually independent sets of equipment. Each includes a general purpose digital computer, a communications buffer, and input/output peripheral equipment.

The two computers in the system are the scientific data systems, SDS 910 and SDS 920. These features are incorporated in both machines:

(1) 8192 words of addressable core memory.

(2) Y-buffer containing a 24-bit word register and 6-bit character register.

(3) Power fail-safe assembly to preserve the contents of internal machine registers in the event of power failure.

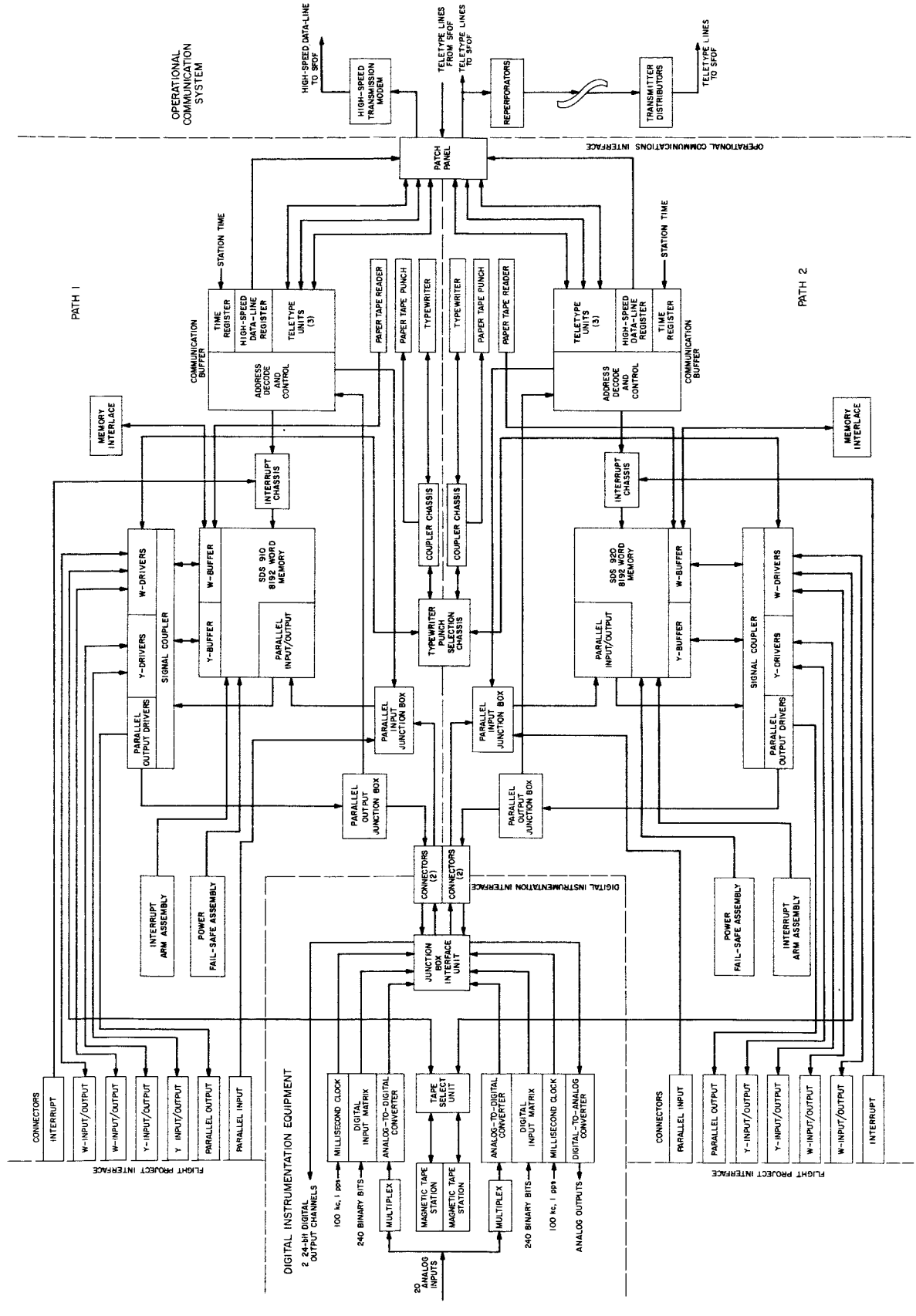


Fig. 10. Deep Space Network data processing system block diagram

(4) Priority interrupt assembly to provide 16 additional priority interrupt channels.

(5) Interrupt arming assembly to permit the selective turn-on and turn-off of priority interrupts under program control.

(6) Signal coupler chassis to provide remote location line driving capability.

(7) Memory interlace unit to facilitate block data transfers between the computer memory and external equipments.

A communications buffer is attached to the parallel input/output channel of each computer. Both buffers are identical; each incorporates a time register, three teletype (TTY) units, and a high-speed data register. The time register provides day of year and time of day in GMT hours, minutes, and seconds. The TTY units are used to send and receive data over teletype lines. The high-speed data register sends data over high-speed data lines.

The following input/output peripheral equipment is provided with each computer:

(1) Input/output typewriter.

(2) Paper tape (Mylar) punch.

(3) Paper tape (Mylar) reader.

(4) Paper tape spooler.

(5) Magnetic tape station.

Identical sets of connectors are provided on each computer to interface with special purpose flight project equipment, and a patch panel is provided for interconnection of teletype and high-speed data lines.

The duplicate sets of equipment described here are configured to provide two on-line data processing paths. Path 1 includes the SDS 910 and its associated buffering and peripheral equipment. Path 2 includes the SDS 920 and its associated buffering and peripheral equipment. The system may be configured in either one of two nominal operating modes and two backup modes. The four modes are indicated in Table 1. Briefly, Mode IA is the nominal station instrumentation mode with full instrumentation data processing capability; Mode IB is the backup instrumentation mode with limited instrumentation data processing capability; Mode IIA is the nominal flight project support mode with single mission telemetry and command data processing capability and limited instrumentation data processing capability; Mode IIB is the backup flight project support mode with single mission telemetry and command data processing capability.

Table 1. On-site data processing system operating modes

Mode	Path	Functions
IA	1	Gather, monitor, and record station instrumentation data
	2	Analyze station instrumentation data
IB	1	Inoperative
	2	Gather, monitor, and record station instrumentation data
IIA	1	Process telemetry and command data for one mission
	2	Gather, monitor, and record station instrumentation data
IIB	1	Inoperative
	2	Process telemetry and command data for one mission

IV. DSN Ground Communication System

A. High-Speed Data Communications System

1. Introduction

The need to transmit telemetry data which has been received at Deep Space Instrumentation Facility (DSIF) stations from advanced spacecraft at relatively high bit rates to the Space Flight Operations Facility (SFOF) for real-time analysis has generated a requirement for the development of a Deep Space Network (DSN) high-speed data communications system.

Binary digital data can be transmitted at very high rates provided that sufficient bandwidth is available in the transmission facilities and sufficient signal-to-noise power ratio can be maintained. However, wide-band transmission facilities are costly and limited in availability in many areas and totally unavailable in other areas of the world in which DSIF stations are located. Voice-grade communications circuits with nominal 3-kc bandwidths are, however, generally available nationally and can normally be provided internationally. Therefore, development of the DSN high-speed data communications system has been based on the utilization of nominal 3-kc circuits.

2. Data Transmission Capabilities of Voice-Grade Communication Circuits

Nominal 3-kc voice-grade circuits do not provide a full 3000 cycles of bandwidth which is useful for data transmission. Significant degradation in the amplitude response of such circuits normally occurs at frequencies below approximately 500 cycles and above approximately 2500 cycles. Also, the envelope delay characteristics of typical channels cause significant phase distortion of any signals in the frequency band below approximately 300 cycles and above approximately 2500 cycles. Thus, the bandwidth of a nominal 3-kc voice-grade circuit which is useful for reasonably satisfactory data transmission is limited to approximately 1700 cycles. Amplitude and delay equalization techniques can be utilized to specially condition 3-kc circuits for data transmission. However, even specially conditioned channels rarely can provide more than 2000 cycles of bandwidth for data transmission.

This information is based on voice-grade communication circuits which are available within the United States. Much less specific information is available regarding the extremely long (up to 10,000 mi) transmission facilities composed of both national and international circuits which are necessary in the DSN operational communications system. It can be anticipated that the characteristics

of such long and varied circuits will cause further reduction of the useful data transmission bandwidth to as little as 1200 cycles.

It is apparent that some form of modulation is necessary to place the information to be transmitted within the useful spectrum of available transmission facilities. Various types of high-speed data transmission terminal equipment are produced which utilize amplitude, frequency, or phase modulation of a carrier signal to convey the information over a voice-grade circuit. The choice of a particular modulation technique for any practical communication system can be difficult and must be highly dependent on the particular characteristics of available transmission facilities, desired transmission rates, and acceptable error tolerances.

Equipments which utilize phase-shift keying (phase modulation) with differentially coherent detection, frequency-shift keying (frequency modulation) with noncoherent detection, and vestigial sideband amplitude modulation with synchronous detection were considered in the selection of the high-speed data communications terminal equipment for the DSN system. The differentially coherent phase-shift keying system was ultimately selected.

3. General Description of Terminal Equipment

The high-speed data transmission keyers and receivers which are being procured for the DSN system are manufactured by the Hallicrafters Co. Two basic types of equipment will be installed in the system. Type I equipment is capable of operation at any of the following switch-selectable data transmission rates: 137.5, 550, 600, 1100, 1200, or 2400 bits/sec. Type II equipment is functionally similar but capable of operation at 2200 or 4400 bits/sec over appropriate transmission facilities. The actual usable transmission rate may be limited below the maximum capability of the terminal equipment by the characteristics of available circuits. The rates of 600, 1200, and 2400 bits/sec are those which have been established as standard in the communications industry, while the rates of 137.5, 550, 1100, 2200, and 4400 bits/sec are nonstandard and were specially incorporated in the JPL equipment to provide support of the *Surveyor* Project.

The transmission keyer (transmitter) units utilize 180-deg phase-reversal modulation of a carrier signal and a special data coding translation technique. The coding translation technique permits the transmission of purely random input data as particularly chosen, restricted combinations of logic *ones* and *zeros*. It is therefore unnecessary to apply any restrictions on the possible combinations of *ones* and *zeros* in the input data to maintain synchronism between a keyer and a receiver. The transmission receivers employ synchronous detection and differentially coherent phase comparison techniques.

4. Description of Transmission Keyer Units

The basic timing control for the transmission keyers is provided by a stable 76.8-kc crystal oscillator. The output of the crystal oscillator is divided to the required frequencies for the carrier signal, 9-bit timing, and bit-rate timing. The various frequencies required for each of the basic bit rates are listed in Table 1.

Table 1. Frequencies required for each basic bit rate

Bit rate, cps	Transfer or sync, cps	9-bit timing, cps	Carrier, cps
137.5	27.5	247.5	1980
550	110	990	1980
600	120	1080	2160
1100	220	1980	1980
1200	240	2160	2160
2200	440	3960	1980
4400	880	7920	3960

Actual data timing either can be accepted from an external timing source or be provided by the keyer to the external equipment. A switch is provided to select the mode of timing to be utilized. When external data timing is selected, the external clock signal is compared with the local crystal oscillator clock and any phase difference between the two clock signals will cause dividers to reset until the local clock is in phase with the external signal. The keyer timing generation block diagram is shown in Fig. 1.

Fig. 2 is a block diagram of the keyer (transmitter modem) and Fig. 3 is an illustration of typical keyer waveforms corresponding to numbered locations in the block diagram.

A keyer will accept specified logic levels of input data in nonreturn-to-zero (NRZ) format in groups or blocks of any length and at any of the specified data rates. The input processing circuits provide necessary level conversion and waveform restoration. The input data is loaded into a 5-bit register which is clocked at the data

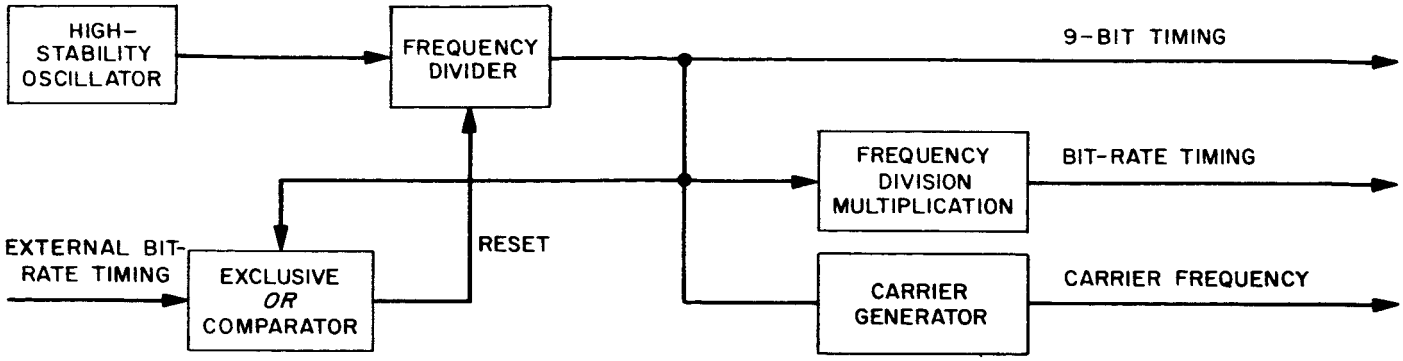


Fig. 1. Timing generator–transmitter block diagram

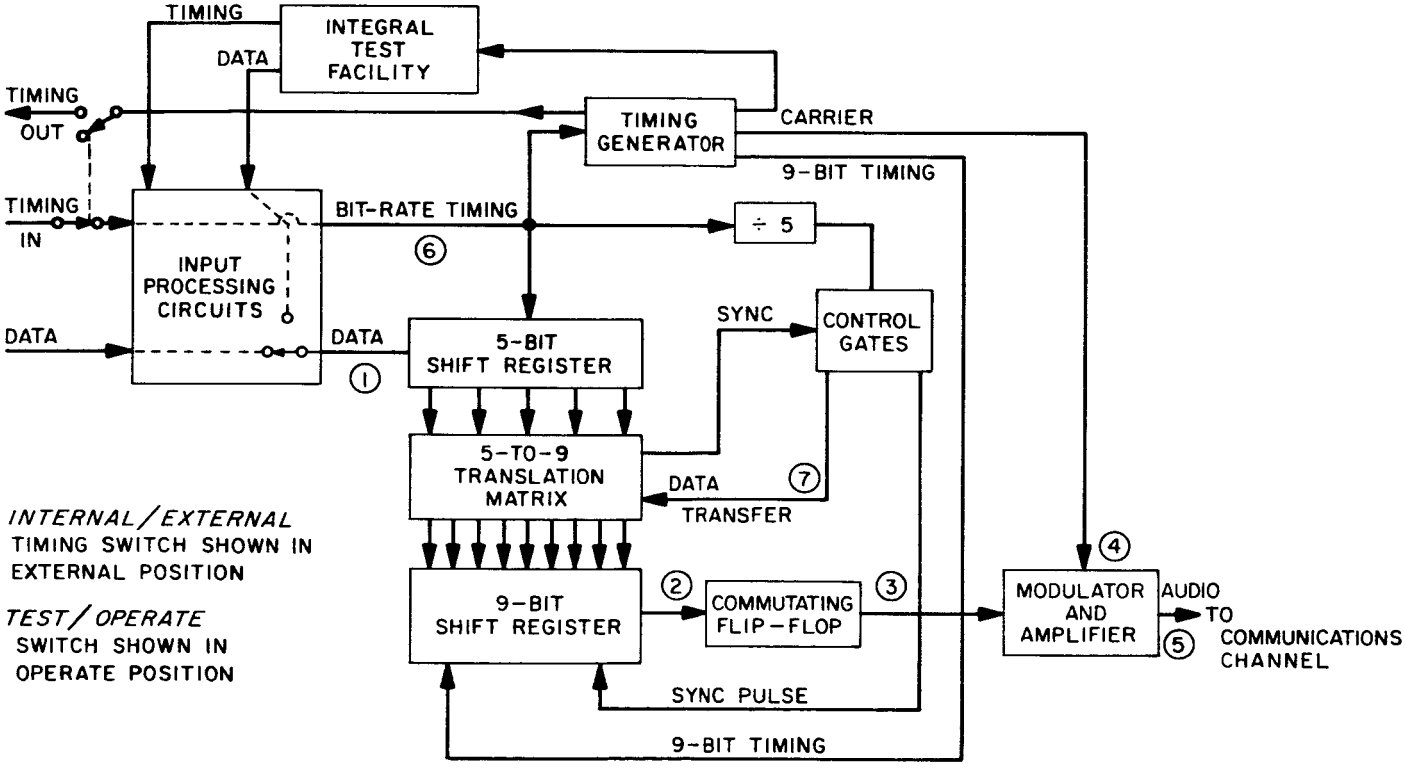


Fig. 2. Transmitter block diagram

rate. Data is transferred from the 5-bit register to the 5-to-9 translation matrix at 1/5 of the input rate. For each of the 32 possible combinations of 5-bit groups of input data, the 5-to-9 translation matrix produces a unique 9-bit code group. Such groups are restricted to those which contain combinations of *ones* and *zeros* which are statistically less susceptible to errors in transmission.

The output of the translation matrix is transferred to a 9-bit shift register which is clocked at 9/5 of the input data rate. The continuous output data stream of that register is applied to a *ones* crossover or commutating flip-flop which changes state only on the trailing edge of logic *ones* in the data stream and provides an output to the phase-reversal modulator. Thus, logic *ones* in the 9-bit data patterns cause a 180-deg phase reversal of the carrier signal.

The phase-reversal modulated carrier is then amplified and filtered to provide compatibility with the bandwidth and level requirements of the voice-frequency communication circuit. The output filter attenuates signal components below 900 and above 2200 cps. An output

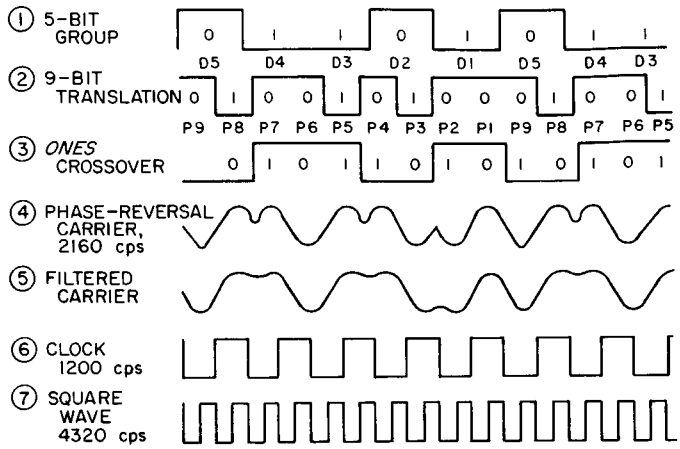


Fig. 3. Typical transmitter waveforms

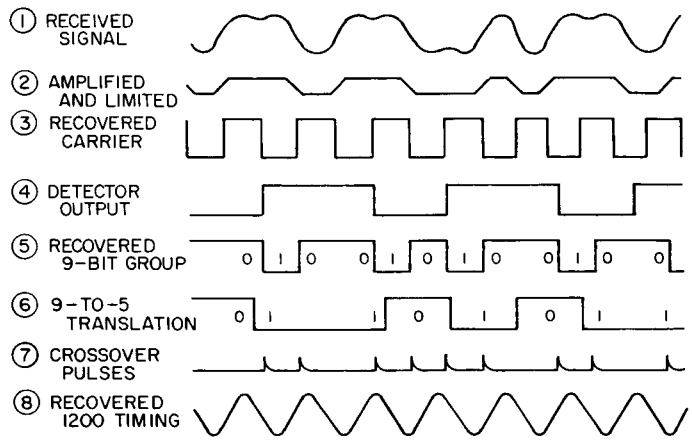


Fig. 5. Typical receiver waveforms

attenuator provides for adjustment of the output signal level between −15 and +15 dbm in 3-dbm steps.

5. Description of Transmission Receiver Units

A block diagram of a transmission receiver unit (receiver modem) is shown in Fig. 4 and typical receiver waveforms corresponding to numbered locations in the block diagram are shown in Fig. 5.

At a receiver, the phase-reversal modulated audio-frequency carrier signal from a communications circuit is applied to the input conditioning circuit which provides a relatively constant amplitude signal to the detector despite input level fluctuations due to circuit degradation of as great as +15 to −40 dbm.

The input signal is then applied to the synchronous detector and to the carrier recovery doubler and filter circuit. The doubled carrier frequency output of that circuit is divided by a flip-flop and applied to the detector as the differential phase reference. The detector effectively generates a *one* when its two input signals are out of phase and a *zero* when the signals remain in phase.

The dc-level variations in the detector output thus represent detected phase reversals and are filtered and

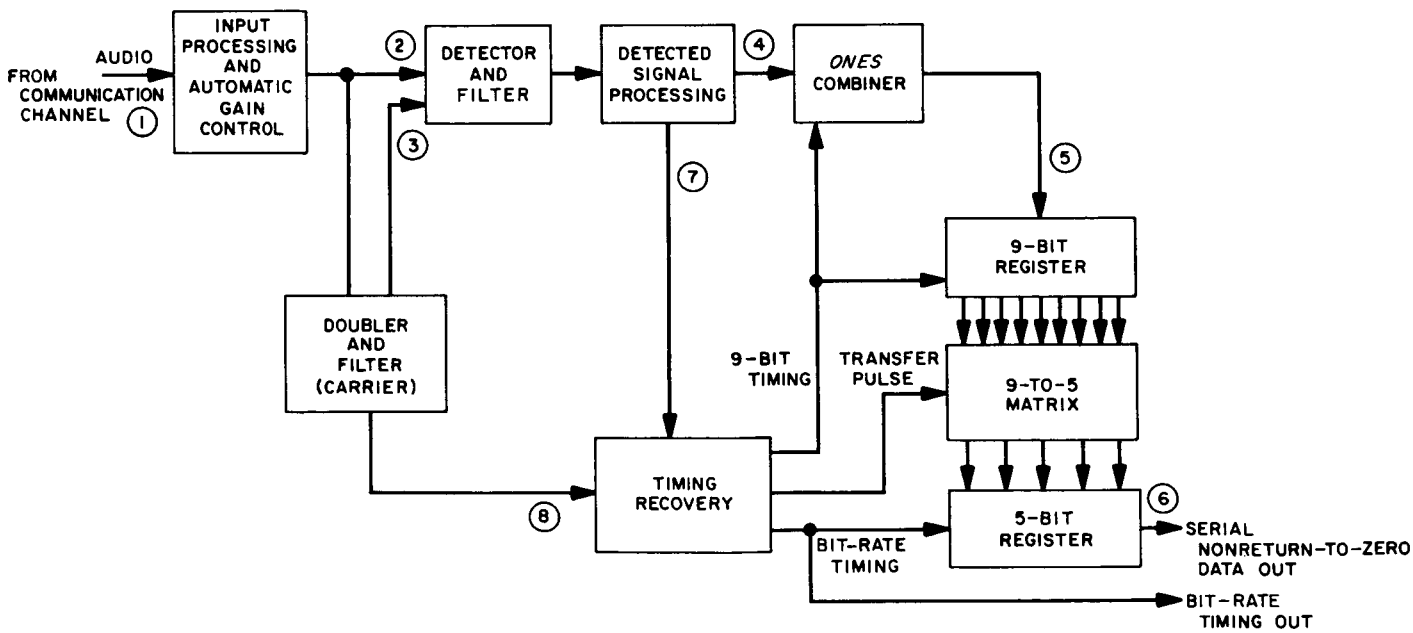


Fig. 4. Receiver block diagram

applied to a slicer circuit for squaring. The slicer circuit provides auxiliary pulse outputs which are functions of the phase reversals in the input data stream and are used to provide a reference for correcting internal receiver timing.

A block diagram of a receiver timing recovery circuit is shown in Fig. 6. The carrier square-wave output of the carrier recovery doubler and filter circuit and the auxiliary pulse outputs of the detector slicing circuit are used to phase-lock the local clock oscillator output to the received data-rate timing. The local clock then provides the 9-bit timing signal, the bit-rate timing for internal receiver functions, and an output bit-rate clock signal which is available for synchronization of external equipment with the output data stream.

The detector data output is applied to a *ones* combiner circuit and then loaded into a 9-bit register. Nine bits of received data are transferred to the 9-to-5 translation decoding matrix. The 5-bit parallel output of the matrix corresponds to the original 5-bit input group at the transmission keyer. The 5-bit register is clocked at the selected bit rate to provide a continuous, serial NRZ data stream to external equipment.

6. Integral Test Facility

The transmission keyers and receivers are equipped with integral test facilities (ITF). Block diagrams of both the keyer and receiver portions of the ITF are shown in Fig. 7. During periods when the equipment is not transmitting operational data, the units can be placed in the test mode by manually actuating a front panel OPERATE/TEST switch. The ITF will operate at any of the selectable bit rates. When a keyer unit is placed in the test mode, the ITF provides a repetitive 80-bit pattern of known coding to the keyer input circuits. At the associated receiver, the incoming test pattern is processed and applied as NRZ data to a comparator circuit. The comparator circuit also receives an input from a local 80-bit pattern generator of identical coding to that of the keyer unit, which is synchronized with the keyer ITF.

The error output pulses of the receiver ITF comparator are integrated to illuminate a front panel lamp at discrete error rates and are available for use with an external counter or other error monitoring equipment. It is anticipated that the ITF capability will be most useful for aligning and evaluating system operation.

7. Over-All System Configuration

In the initial configuration of the DSN high-speed data communication system, at least one transmission keyer will be installed at each DSIF station, in JPL facilities at the Atlantic Missile Range (AMR), in the Spacecraft Assembly Facility (SAF), in the SFOF, and one unit will be available for installation at major spacecraft contractor

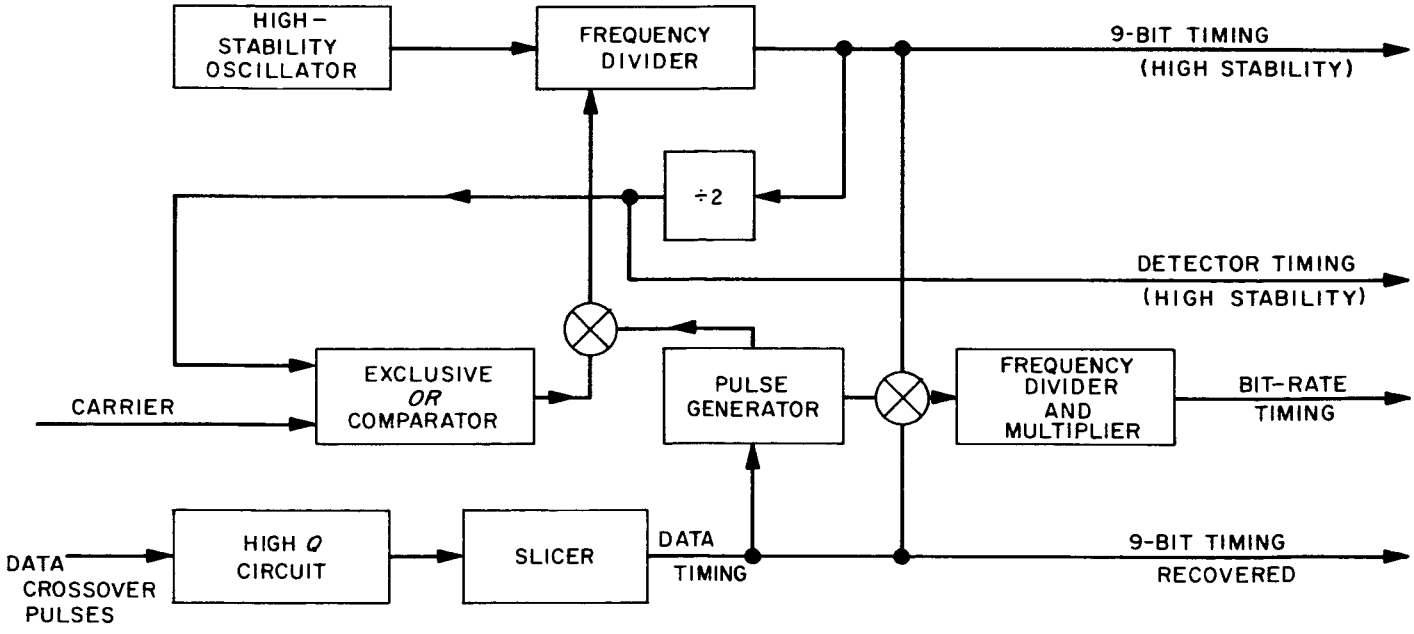


Fig. 6. Recovered timing–receiver block diagram

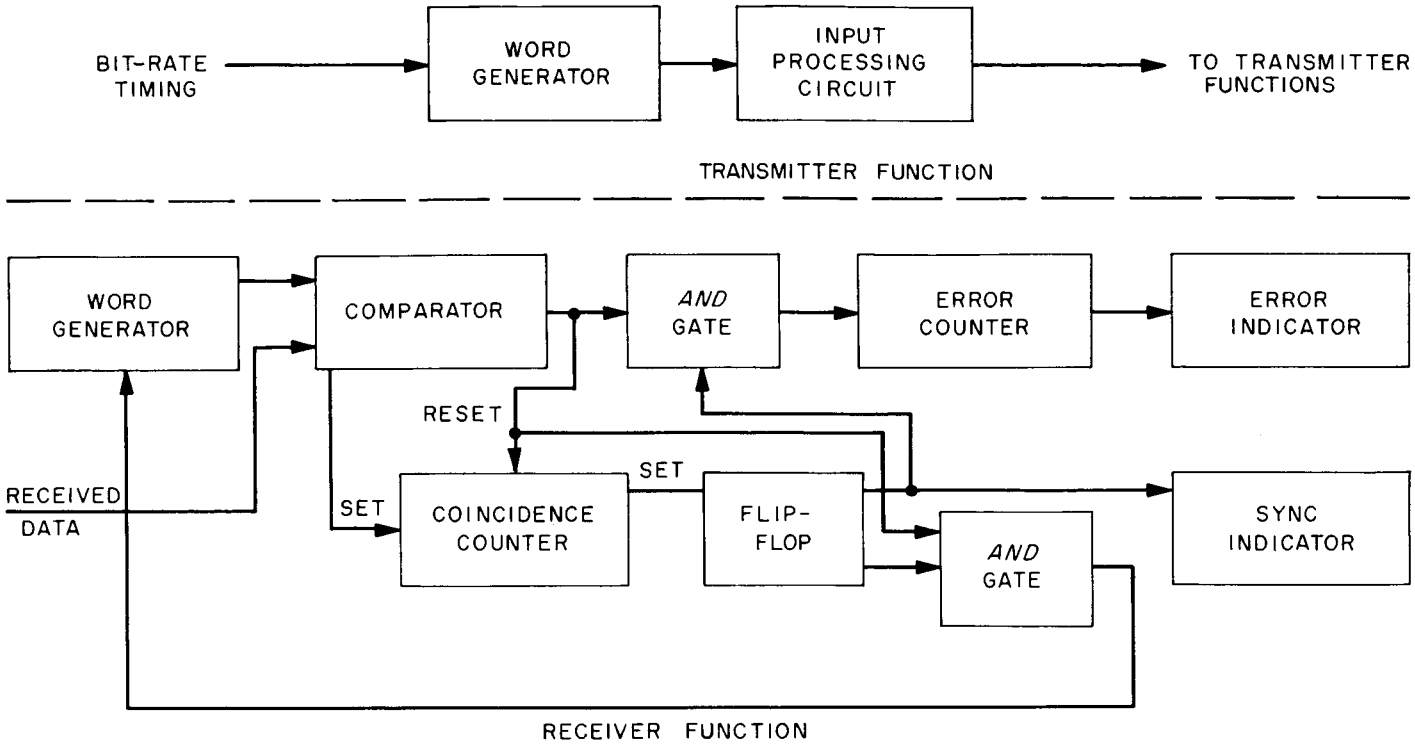


Fig. 7. Integral test facility block diagram

facilities. In those cases where a second unit is installed at a DSIF station, the second unit will be an operational spare. Three Type I receivers will be installed at the SFOF and one at Goldstone DSIF. One Type II transmission keyer will be installed at the Goldstone Pioneer DSIF site and a corresponding Type II receiver will be installed at the SFOF. The latter units will utilize a 6-kc program channel of the Pasadena–Goldstone microwave system at the transmission facility. Five line equalizer units will also be installed at the SFOF to provide a means of improving the data signal conditioning of circuits derived from facilities other than the microwave system.

A special circuit or system configuration will be utilized for high-speed data communication from the DSIF site at Johannesburg, South Africa. This special configuration is required because it is necessary to utilize high-frequency radio as the transmission medium for a major portion of that circuit. The inherent characteristics of high-frequency radio paths place significantly greater limitations on high-speed data communications capability and reliability than is the case with nominal landline or microwave facilities. A standard Type 1 keyer will be installed at the DSIF station and a circuit derived from landline facilities will be utilized for transmission to the South African radio terminal at Deterpoort. A Type I receiver will be installed at the radio terminal. Output of the receiver will pass through serial-to-parallel conversion equipment.

Conventional frequency division multiplex (FDM) equipment will accept the parallel data stream and provide frequency-shift keying of the high-frequency radio transmitter. At a serial rate of 600 bits/sec, which will be the maximum available rate on this circuit, 8 parallel channels of the FDM equipment will be utilized in the radio path to reduce the individual channel rate to 75 bits/sec. The high-frequency radio system will be routed via a relay station at Tangiers, Morocco, to the receiving station in New York.

At New York, conventional FDM receiving equipment will be utilized to provide a parallel bit stream output to a parallel-to-serial converter. The serial converter output is applied to the input of a standard JPL Type I transmission keyer and the transcontinental portion of the circuit is functionally identical to other landline circuits.

All of the incoming data circuits terminate at the SFOF communications terminal equipment room. A block diagram of the internal SFOF high-speed data communications subsystem is shown in Fig. 8.

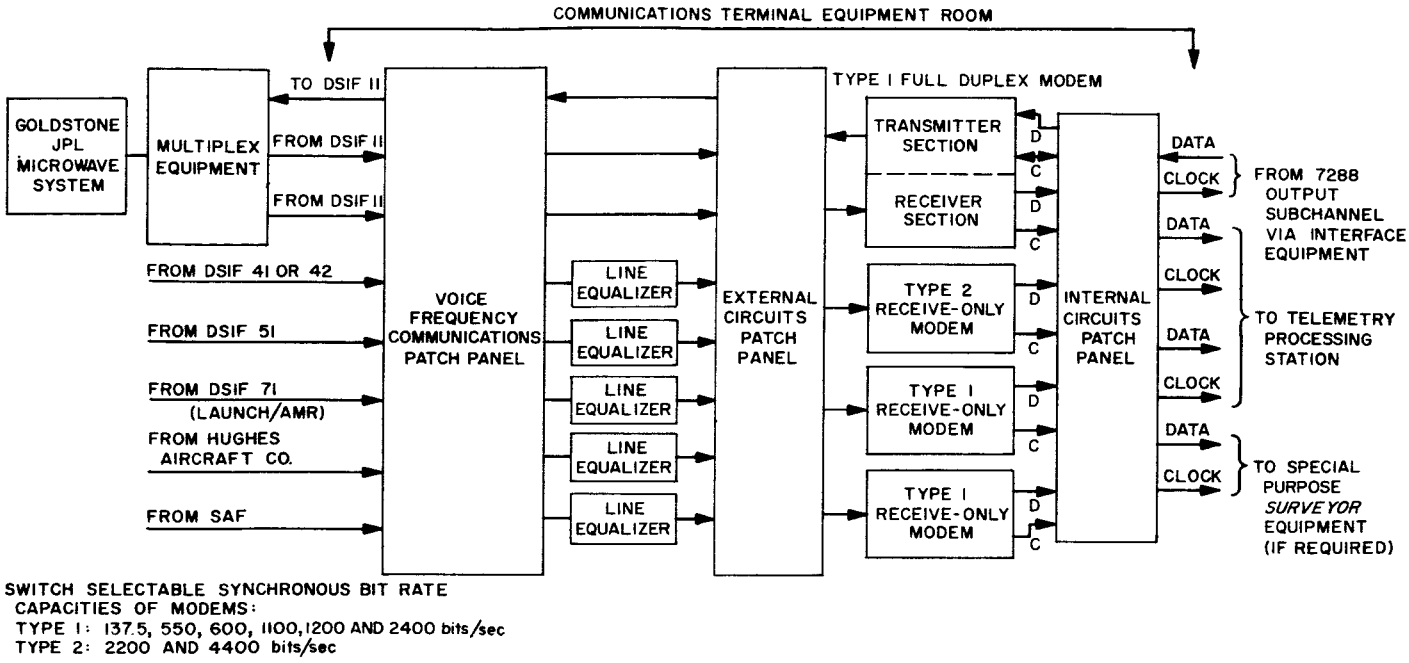


Fig. 8. SFOF high-speed data communications subsystem

V. Communications Engineering Developments

A. S-Band Implementation for DSIF

1. TWM for DSIF

Summary. The prototype traveling wave maser/closed cycle refrigerator (TWM/CCR) at the Venus site was modified to use a new direct-drive motor which eliminates all gears in the CCR crosshead drive. This recent development is expected to provide increased reliability and less frequent maintenance. The electrical performance of the TWM/CCR systems delivered thus far satisfies the specified requirements.

The program to install traveling wave masers in the DSIF is well under way. The first system was shipped to the Johannesburg Station and a second system is now being readied for shipment to the Woomera Station. The system for the Pioneer Station is also near completion.

One shortcoming of the A. D. Little Co. closed cycle refrigerators used with the S-band traveling wave maser system has been in the crosshead drive mechanism which used a set of speed-reducing gears. A small pinion gear has been known to fail, unpredictably, after periods varying from a few hundred hours to a few thousand hours. An expected solution to this problem evolved in two steps described here.

First, it was necessary to demonstrate that the pistons in the CCR could be driven sinusoidally, rather than with the square-wave motion designed into it, without serious loss of performance. This proved to be the case as shown experimentally at JPL and A. D. Little Co. Once this was shown, it was necessary to provide a slow-speed motor with adequate torque. Induction motors, unfortunately, become bulky and inefficient when designed for low speeds.

A relatively recent development by the Superior Electric Co. has appeared at an opportune time. This is a slow speed synchronous motor with high torque. Called a "synchronous inductor motor," the machine uses a permanent magnet rotor with a gear-tooth configuration. The stator is similar to that of a four-pole induction motor except that the pole pieces are machined like the rotor with many toothed projections. The number of teeth in the stator and rotor are different, however, and are so

chosen that the rotor advances 1 tooth/cycle of the applied voltage; with a 50-tooth rotor a speed of 72 rpm is obtained. The torque developed is more than adequate (400 in.-oz) in a unit which is only slightly larger than the original motor. Plans are to retrofit all stations with the new drive motor as soon as they become available.

The electrical performance of the two TWM/CCR systems delivered to date is summarized and compared with the original specifications in Table 1. Four systems remain to be delivered; they are in various stages of construction and test.

2. Acquisition Aid for DSIF

Summary. As part of the DSIF S-band implementation project, an S-band acquisition aid (SAA) is being developed for the 85-ft antennas. The first system, ultimately to be installed at Canberra, Australia, has been installed and qualitatively evaluated at the Goldstone Pioneer Station; the second system has been shipped to the Woomera Station, Australia, and the third system is scheduled for shipment to Johannesburg, South Africa, early in May.

The first S-band acquisition aid system, described in Ref. 1, has been installed and qualitatively evaluated at the Pioneer Station using the L-S three-channel receiver system. The VSWR performance, as measured at the electronics cage interface, is shown in Table 2.

Time has not yet permitted a detailed study of the SAA boresight stability, although one of the major contributing factors, boresight shift with reference-to-error channel phasing, has been measured. This effect is found to be ± 0.045 deg for ± 30 min phasing error (either error channel) indicating an operational null depth of 37 db.

Table 2. VSWR performance[a]

Port	VSWR, center frequency	VSWR, 10-Mc band
Receiver, reference channel	1.04 (2295 Mc)	≤1.20
Receiver, error channel	1.15 (2295 Mc)	≤1.6
Transmitter	1.13 (2115 Mc)	≤1.16

[a]Maximum, either polarization.

Helicopter tests, utilizing the L-S receiver, were performed March 31 through April 8. No significant problems were encountered either in acquisition or antenna switchover. A preliminary helicopter test, utilizing the six-channel S-band receiver, was conducted April 10. Qualitatively successful performance was obtained; further boresight alignment studies are presently being conducted to improve SAA to 85-ft-aperture antenna switchover characteristics.

3. Microwave Switch Control Assembly

The first microwave switch control assembly for the DSIF S-band system (Ref. 2) has been installed at the Pioneer Station and is presently undergoing tests and operational evaluation. At this time there are no known performance deficiencies. It will take several months of actual operation to determine whether the functional design and operational concept will allow easy, unambiguous operation by station personnel.

To date, three microwave switch control assemblies are complete, the one for Pioneer described above, and those for the Johannesburg and Woomera Stations which have been packaged and are in transit to their respective sites. The remaining two systems will be complete by May 15, 1964.

Table 1. Performance of TWM/CCR systems (Laboratory tests prior to shipment to GTS)

Item	Specifications	Johannesburg system	Woomera system	Pioneer system
Gain (at 2295 Mc)	30 ±1 db	36 ±1	35 ±1	36 ±1
Bandwidth (3-db points)	15 Mc	18 Mc	16 Mc	17 Mc
Bandwidth (1-db point)	10 Mc	10 Mc	10 Mc	10 Mc
Tunable range	±30 Mc	+10, −20 Mc	+10, −20 Mc	+10, −20 Mc
Input noise temperature	16°K ±2	9°K ±1	10°K ±1	9°K ±1
Gain stability:				
Short term	±0.02 db in 10 sec	±0.015 db	±0.02 db	±0.025 db
Long term	±0.2 db in 12 hr	±0.2 db	—	±0.2 db
Tilt test 180 deg		±0.2 db	±0.3 db	±0.25 db

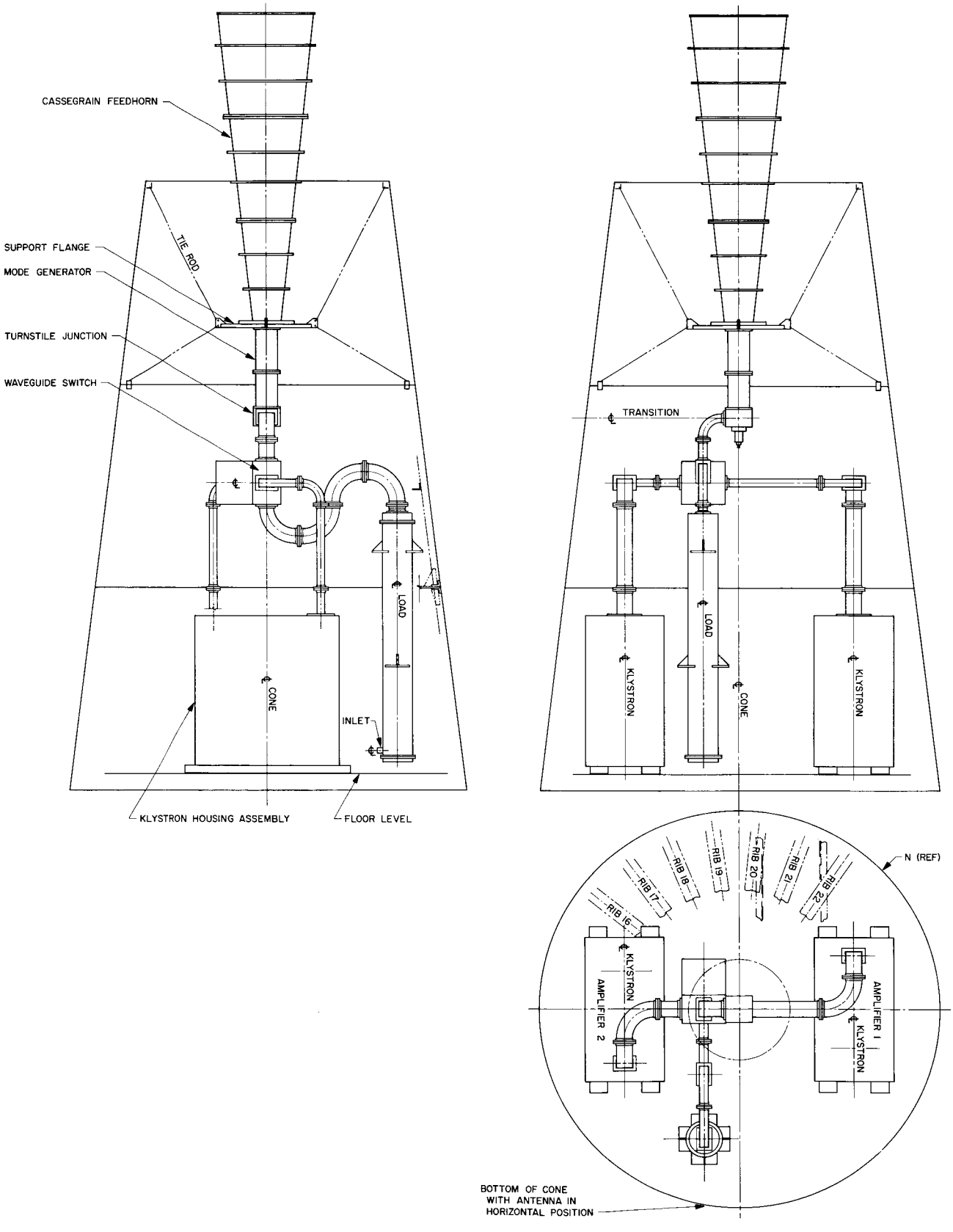


Fig. 1. Final layout in Cassegrain feed cone

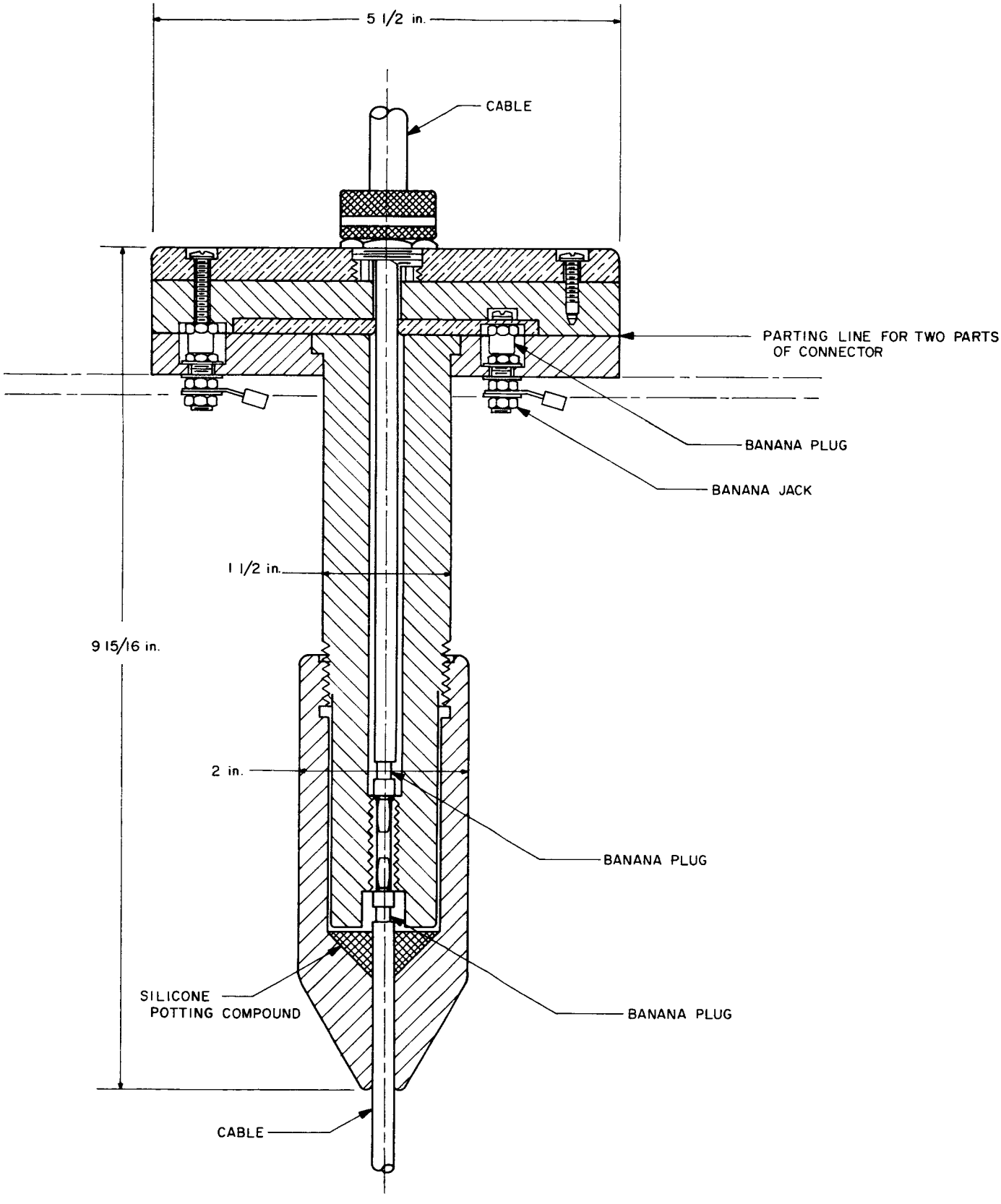


Fig. 2. Sectional view of high-voltage connector

B. *Mariner* C Transmitter Development

1. Mariner C 100-kw Transmitter

a. Introduction. Under certain operating conditions, it has been determined that a ground transmitter power of 100-kw continuous wave (CW) will be required for the *Mariner C* program. The complete transmitter program to meet this requirement consists of a 100-kw klystron amplifier subassembly, a ground test and checkout facility and specialized controls for this installation.

b. Klystron amplifier subassembly. As stated in Ref. 3, the assembly of the amplifier subsystem is under contract with Energy Systems, Inc. The contractor's effort is on schedule and the delivery of the amplifier subsystem to the Venus site is scheduled for June 1, 1964. The amplifier layout in the Cassegrain feed cone has been finalized and is shown in Fig. 1. The layout has been designed, using standard waveguide components, up to the turnstile junction to assure ease of replacement and reproducibility. The items from the turnstile junction on through the feedhorn are furnished by JPL to the contractor for installation.

In Ref. 4 it was indicated that the high voltage to the klystron would be transferred from one amplifier to the other by means of a switch. During the final layout of the feed cone described above, there was not sufficient room to install a high-voltage switch. In order to transfer the high voltage from one amplifier to the other a high-voltage connector has been developed, a sectional view of which is shown in Fig. 2. The connector has been designed so that the inner and outer shield are connected at the same time as the center high-voltage conductor. A microswitch is installed on one of the guide pins for the connector in such a manner that the high-voltage interlock will be opened and the voltage removed before the high-voltage connection in the connector is interrupted.

References

1. "Acquisition Aid for DSIF," *SPS 37-26*, Vol. III, p. 62, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

2. "DSIF Microwave Switch Control Assembly," *SPS 37-25*, Vol. III, pp. 53–57, Jet Propulsion Laboratory, Pasadena, California, January 31, 1964.

3. "Klystron Amplifier Subsystem," *SPS 37-26*, Vol. III, p. 22, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

4. "Klystron Amplifier Subsystem," *SPS 37-25*, Vol. III, pp. 18 and 19, Jet Propulsion Laboratory, Pasadena, California, January 31, 1964.

VI. Communications Research and Development

A. Ground Antennas

1. Antenna Instrumentation

A transportable instrumentation system is being developed for use in research and development testing of the structural and mechanical properties of large ground antennas. It is being used initially on the 30- and 85-ft antennas, and later on the 210-ft-D advanced antenna system (AAS). There is a detailed description of the instrumentation system in Ref. 1, and progress reports appear in subsequent issues. Additional equipment was added to the system prior to the latest series of field tests on the 85-ft Az-El antenna (January and February, 1964). The current block diagram of the antenna instrumentation system is shown in Fig. 1. Details of the latest tests are covered in Ref. 2; reduction of the data obtained is continuing. Being designed is a general data reduction program for use with the specific data system which provides low-speed data sampling on punched paper tape records. The program will enable rapid reduction of data from future tests.

2. Radio Calibration Techniques

Radio astronomical techniques have been employed at the Venus site for the calibration of the 85-ft Az-El antenna which has been calibrated for pointing accuracy and effective antenna area by using the signal received by several intense radio sources. Boresight measurement procedures have been described in Refs. 3, 4, and 5; measurement of effective antenna area and antenna gain are described in Refs. 4, 6, and 7. In measuring radiometric quantities, radio-frequency terminations immersed in a cryogenic bath are employed as thermal noise standards.

Recently the Cassegrainian cone was removed from the Venus site 85-ft antenna to facilitate antenna structural measurements. During that time, the insertion loss of the cone transmission line was measured and evaluation of the cryogenic loads was performed. The insertion losses were reported in Ref. 8. Revised values of the cold load temperatures are presented. Preliminary results of minimum antenna temperature (11°K), temperature versus elevation angle, and radio-source gain measurements are presented.

The cryogenic loads used as thermal power standards in the Venus site radar receiver were recently removed from the Cassegrainian cone and sent back to JPL for recalibration. A direct radiometric calibration of the terminations was performed by comparing the thermal radio-frequency noise output of the test load with that

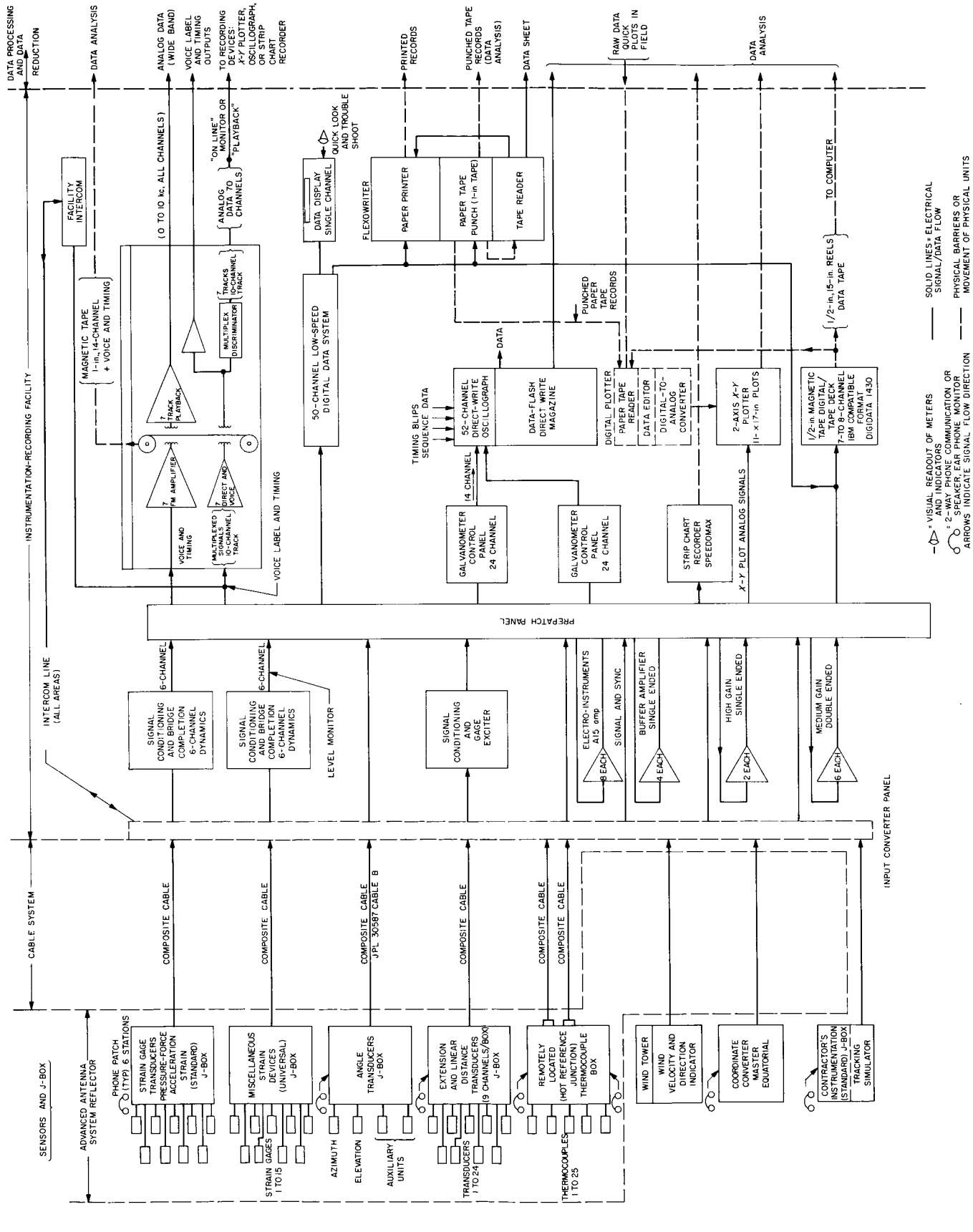


Fig. 1. Antenna instrumentation system block diagram

of a standard WR 430 liquid-helium-cooled waveguide load. The standard waveguide load was similar in design and construction to the load discussed in Ref. 9. The effective output power of the standard load was calculated to be 6.2°K. This was determined by measuring the insertion loss of the WR 430 transmission line and then calculating the output temperature, using the procedures described in Ref. 9.

Upon making direct radiometric comparisons of the cryogenic loads, it was found that the liquid-nitrogen-cooled load displayed a temperature instability as a function of time. This temperature instability was caused by poor mechanical connections in both the load and the transmission line. These poor connections resulted in the load material not being at the same temperature as the cryogenic bath, and in the impedance changing with time. The connections were improved by using indium solder on all low temperature screw joints and using silicon grease to improve the thermal contact between the resistive load and the cryogenic bath.

There were also several poor connections in the helium-cooled load transmission line. These were remedied by lapping all connecting joints.

The cold load measurement and calibration technique is illustrated in Fig. 2. The noise output produced by the standard helium load was compared to the test helium load by switching the waveguide switch between Ports 2 and 3. The difference between the two output levels was calibrated by using a gas tube pulse. The difference between the two loads was found to be 4.6 deg. The symmetry of insertion loss of the two waveguide paths was checked by repeating the measurements with the loads interchanged. The temperature difference was the same within experimental accuracy.

The gas tube temperature was determined by connecting the WR 430 waveguide rotary vane attenuator (Refs. 10 and 11) between a helium load and the switch. The input temperature to the switch is given by:

$$T_1 = T_H + \left(1 - \frac{1}{L_1}\right)(T_0 - T_H)$$

where L_n is the insertion loss ratio, T_0 is the ambient temperature, and T_H is the temperature of the helium. The gas tube was fired and turned off and the rotary vane

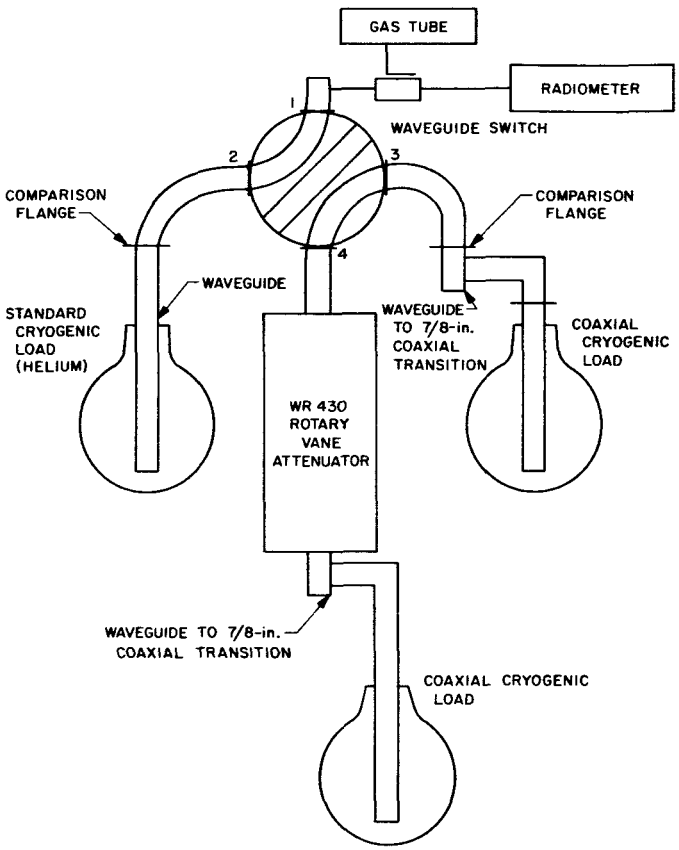


Fig. 2. Diagram of temperature calibration system

attenuator was then adjusted to give the same output level T_2 that was obtained with the gas tube on,

$$T_2 = T_H + \left(1 - \frac{1}{L_2}\right)(T_0 - T_H)$$

The temperature contribution of the gas tube, T_e, is given by:

$$T_e = T_2 - T_1 = \left(\frac{1}{L_1} - \frac{1}{L_2}\right)(T_0 - T_H)$$

The partial derivative of T_e with respect to T_H is

$$\frac{T_e}{T_H} = -\left(\frac{1}{L_1} - \frac{1}{L_2}\right)$$

For the parameters used, any error in T_H will be reduced by a factor of 30 in T_e.

The nitrogen load was calibrated by putting it at Port 2 and the helium load waveguide attenuator at Port 3. The insertion loss necessary to get equal noise

power from Ports 2 and 3 was determined and from this the temperature of the nitrogen load was computed.

The coaxial helium load temperature referred to the waveguide output flange on the transition was found to be 10.8 (+0.9, −0.3)°K and the nitrogen load referred to the waveguide output flange was found to be 85.0 (+1.2, −0.6)°K.

The effective cryogenic load temperatures referred to the maser side of the crossguide coupler were computed by using the ambient temperature and the measured waveguide insertion losses reported in Ref. 8. The effective temperature of the helium load is 14.7 (+1.0, −0.4) °K, and for nitrogen it is 88.5 (+1.3, −0.7)°K. These recently determined values are indicated on the Venus site planetary radar radio-frequency system diagram (Fig. 3).

The ⅞-in. coaxial line gas tube in the Venus site instrumentation has proved to be quite unreliable. It has been replaced with 2 Hewlett-Packard 349A noise sources. One is fired through the waveguide crossguide coupler (Fig. 3) and gives a 25.5 ±0.5°K noise contribution. The second tube has an additional nominal 10-db loss through a directional coupler and gives a noise contribution of 2.25 ±0.1°K.

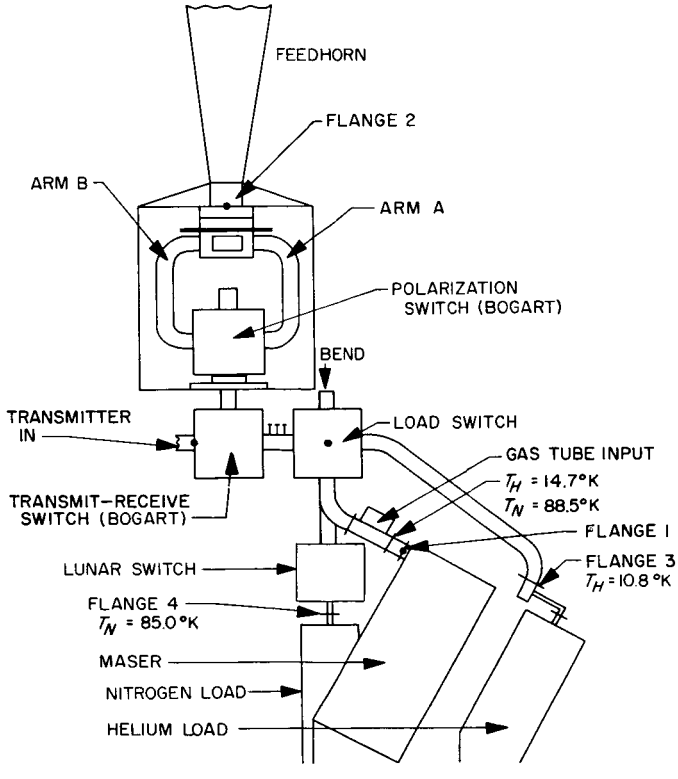


Fig. 3. Recent insertion loss and temperature calibrations of Venus site radio-frequency system

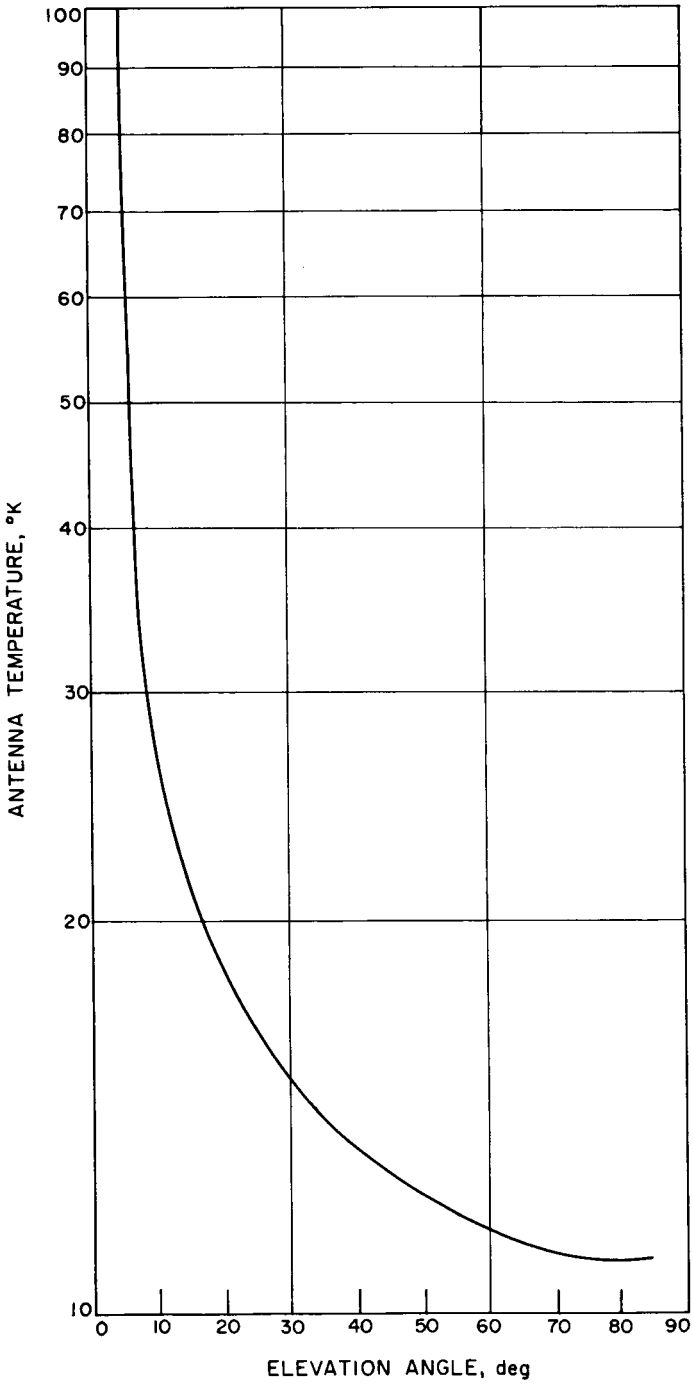


Fig. 4. Antenna temperature versus elevation angle, Venus site 85-ft Az-El antenna (azimuth = 260 deg)

Using these calibrations, the Zenith antenna temperature was measured giving a preliminary value of 11°K. The antenna temperature as a function of elevation angle measured at an azimuth of 260 deg is presented in Fig. 4. The reference point for these measurements is Flange 2, as shown in Fig. 3.

Differential antenna temperatures were measured for Cassiopeia A (186°K) and Cygnus A (100°K). These were both found to be 0.65 ±0.2 db higher than reported in Ref. 6. The increase in gain reported in Ref. 12, believed due to resurfacing the 85-ft antenna, was 0.4 ±0.10 db. Part of the difference may be due to the fact that the surface was adjusted for best performance at 45-deg elevation, but the gain measurements reported in Ref. 12 were made near the horizon.

3. Simultaneous Lobing Radiometric Tracking System

Summary. The S-band systems for the DSIF 85-ft and future 210-ft antennas will use simultaneous lobing angle tracking feed systems. A radiometer which could be used with the tracking feed would be a useful device for angle pointing and gain calibration of the antenna system using radio star sources. An X-band laboratory demonstration model of a simultaneous lobing radiometer receiver channel has been constructed. A noise tube was used to simulate the signal from a radio source. Preliminary experiments have been performed to examine the angle detector output versus reference/error channel differential phase shift and error channel noise-to-signal ratio. This work was described in Ref. 13. The intermediate frequency and direct current components of the demonstration system were recently operated at the Echo site of the Goldstone Tracking Station using the 85-ft antenna and the L-band receiver system. It was possible with an effective system temperature of approximately 500°K to automatically track a radio star which produced an antenna temperature in the reference channel of 5°K; a source which produced a 59°K antenna temperature provided good automatic tracking. Data were taken to evaluate the tracking accuracy; they have not yet been reduced.

a. Equipment. The simultaneous lobing radiometer described in Ref. 13 was improved by the development of a new wide-band phase detector. This new detector employs a wide-band hybrid junction with a nominal bandwidth of 20 to 200 Mc. The hybrid junction is manufactured by Adams-Russel Co. The phase detector block diagram appears in Fig. 5. The electrical characteristics of the phase detector are very similar to those described in Ref. 13; however, the ease of construction and simplicity of adjusting make it more convenient for operational use.

The intermediate frequency (IF) and direct current components of the laboratory radiometer were combined with the input stages of the simultaneous lobing 960-Mc receiver at the Echo Station . The block diagram of this system is illustrated in Fig. 6. The sum channel of the simultaneous lobing feed goes to a parametric amplifier mounted on the antenna apex. The output of the parametric amplifier goes to the sum mixer preamplifier in the antenna electronics cage. The hour angle difference channel goes directly from the feed bridge to a mixer preamplifier in the electronics cage via ⅞-in. coaxial transmission line. Both sum and hour angle mixers used a common 930-Mc local oscillator. The approximate system temperatures of the receiver were: sum channel, 165°K; error channel, 1500°K. The 30-Mc outputs of the mixer preamplifiers are brought down to the control room on coaxial cable. Each channel was amplified in a 30-Mc IF amplifier in the control rooms. The 30-Mc bandwidth was limited to 2 Mc by the mixer preamplifiers. From the sum IF strip the signal went through a delay line which was used as a phase shifter; approximately 15-nsec delay

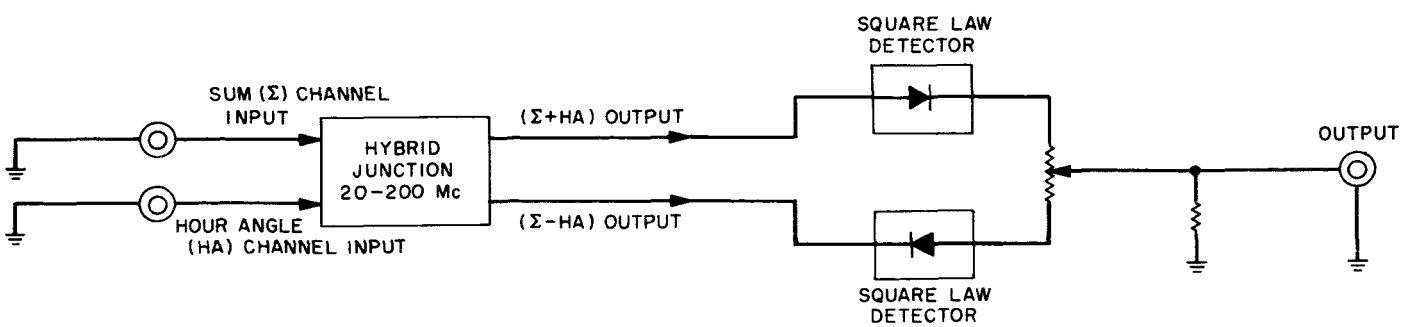


Fig. 5. Phase detector block diagram

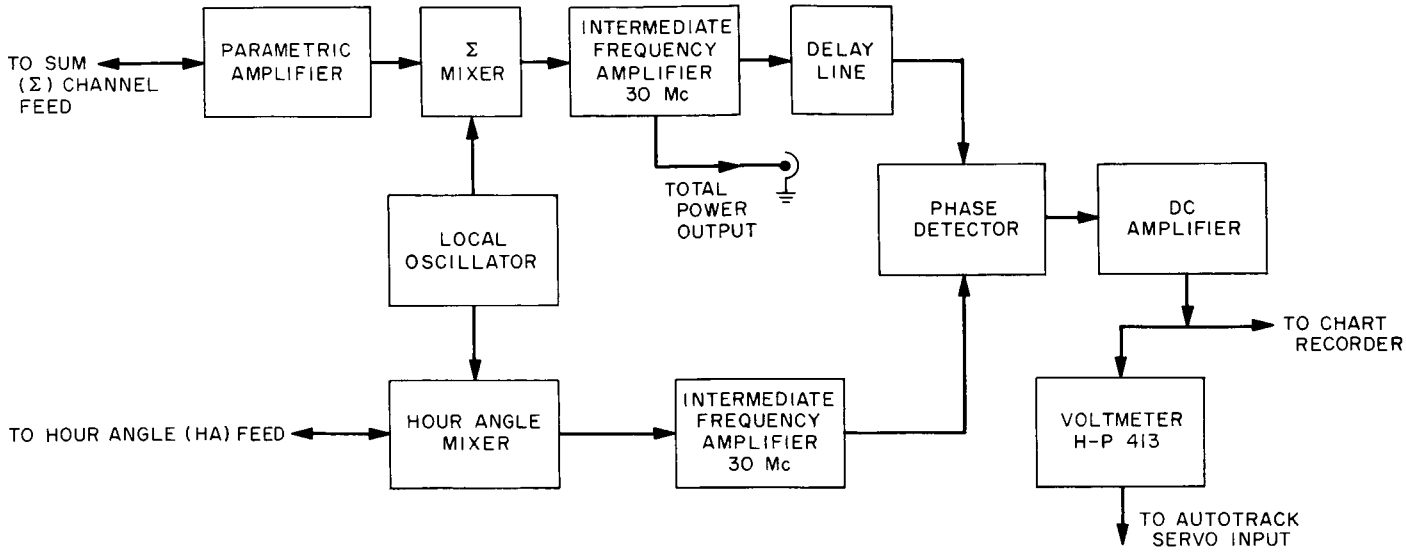


Fig. 6. Simultaneous lobing radiometer autotrack block diagram

was required. The output of the delay line and the difference IF strip went to the phase detector. The output of the phase detector is proportional to the complex product of the correlated noise of both channels. The dc output of the phase detector then went to a dc amplifier which fed a strip chart recorder and a Hewlett-Packard 413 voltmeter. The voltmeter was used to isolate the outputs of the dc amplifier and as a servo error signal input monitor. From the voltmeter the dc error signal was used to control the antenna servo system in automatic tracking mode. Only one angle error channel was available; it was used to control the hour angle axis of the antenna. The declination axis was locked with the brake.

b. Experiments. On the night of April 30–May 1, 1964, the simultaneous lobing radiometer was successfully used on Echo Station's 85-ft antenna to perform automatic radio-frequency (RF) angle tracking of the Crab Nebula, Virgo A, and Hercules A. Fig. 7 shows a drift curve of the Crab Nebula which had an antenna excess noise temperature of about 59°K. The gas tube pulse on the reference channel trace is approximately 100°K. The reference channel trace on the chart is produced from the changes in the total power output of the reference channel as the source drifts through the fixed beam of the antenna. The error channel curve is produced by the output of the phase detector filtered with a 1-sec time constant. The recorder presentation is set up so that 0.5 is the zero output of the angle phase detector. It can be seen that, presumedly due to unbalance, there is an interaction between the gas tube pulse in the reference channel and the phase detector output. Fig. 8 shows a calibration of the phase detector voltage output as a function of offset angle from an ephemeris slave drive on the Crab Nebula. The offset angles were obtained by using the Goldstone Echo Station coordinate converter computer. At the beginning of the run (Fig. 8) a −0.1-deg offset was inserted and the servo was put in autotrack. After this, using the slave drive, offsets with 0.10 increments were inserted to calibrate the detector. After the +0.2-deg offset, the system was put back into autotrack and the system locked on. There is a small difference (≈0.03 deg) between the computed (ephemeris) boresight position and the angle channel phase detector boresight.

Fig. 9 shows a series of servo snap-on tests for which the calibrations of Fig. 8 hold. The servo bandwidth in all but the last snap-on was 0.1 cps; in the last snap-on it was 0.05 cps. For the first snap-on test the antenna was offset west of the source by +0.5 deg, and for the second test it was offset east of the source by −0.5 deg. There was more overshoot from the west offset than the east offset which was believed due to velocity and acceleration differences required for sidereal tracking. The next snap-on had a −0.7-deg offset; the error voltage first increased as the system was placed in autotrack. This was due to the fact that the −0.7-deg offset was past the angle error S-curve maximum. This effect was even more pronounced in the last two runs at −0.9-deg offset. For the last snap-on a 0.05-cps servo bandwidth was used. No serious attempt to optimize the adjustment of the antenna servo response was made in preparation for these tests.

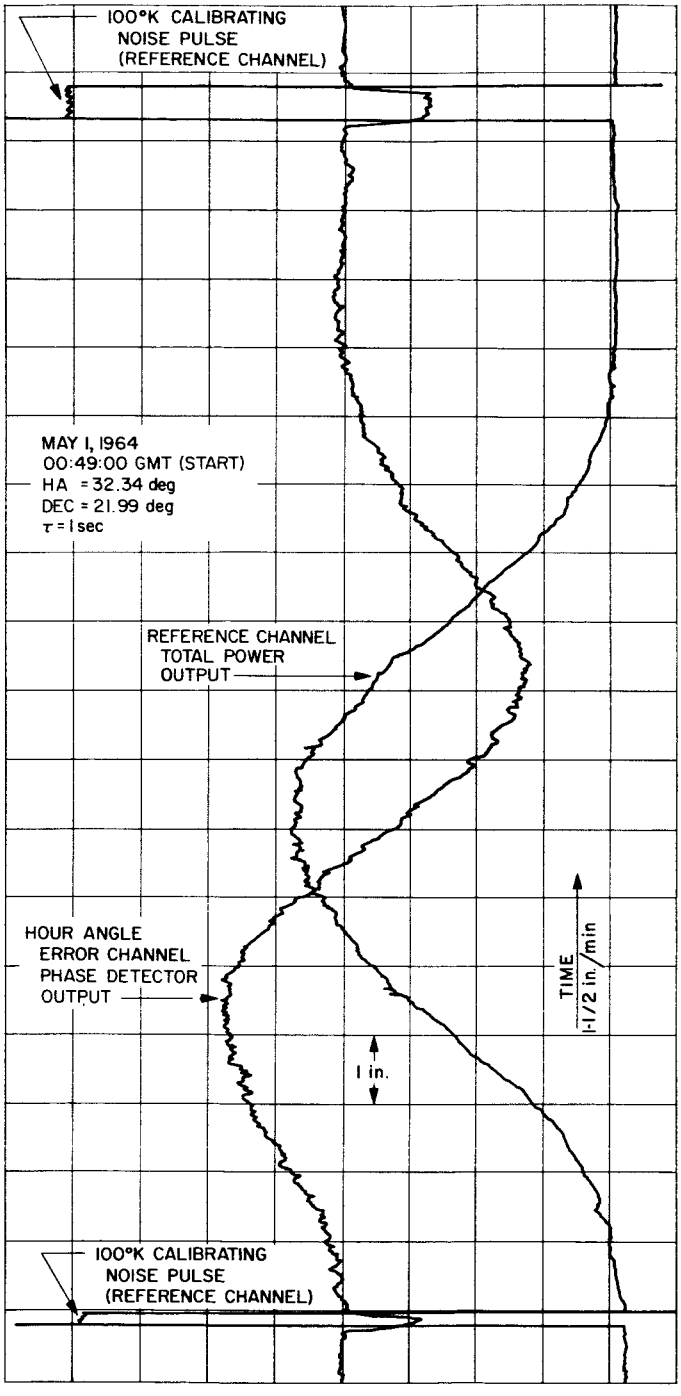


Fig. 7. Total power reference channel drift curve and phase detector output for Crab Nebula

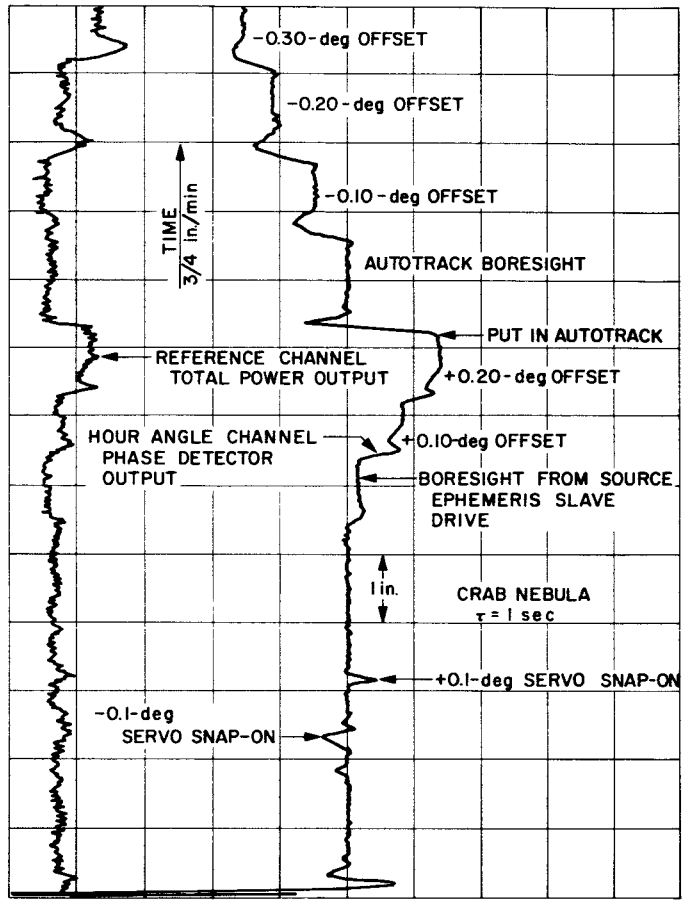


Fig. 8. Phase detector calibration curve

Fig. 10 shows a drift curve for Virgo A which gave approximately a 17°K excess antenna noise temperature. The boresight crossing time as given by the computer is indicated on the record. The gain settings and the constants were the same as for Crab Nebula. Automatic RF angle tracking was readily accomplished on the signal from Virgo A.

Fig. 11 shows a drift curve obtained from Hercules A; for this record, the time constant of the phase detector recording was 5 sec. The approximate excess antenna temperature from the source is 5°K. The source is barely discernible in the sum channel total power output, but a usable angle error S-curve was obtained. Fig. 12 shows +0.5, +0.2, −0.2, −0.5-deg offsets and then a snap-on from −0.5 deg. As noted, only the hour angle channel was used in these preliminary experiments; the declination brakes were kept engaged.

c. Discussion. Manasse, Ref. 14, has shown that for a receiver configuration and a noise-like signal as used in these experiments, the best root-mean-square (rms) angle tracking error one can obtain is given by:

$$\delta\theta = \frac{2}{\pi}\left(\frac{\lambda}{D}\right)\frac{(1 + P_s/P_n)^{1/2}}{(P_s/P_n)\,(2\tau W)^{1/2}} \qquad (1)$$

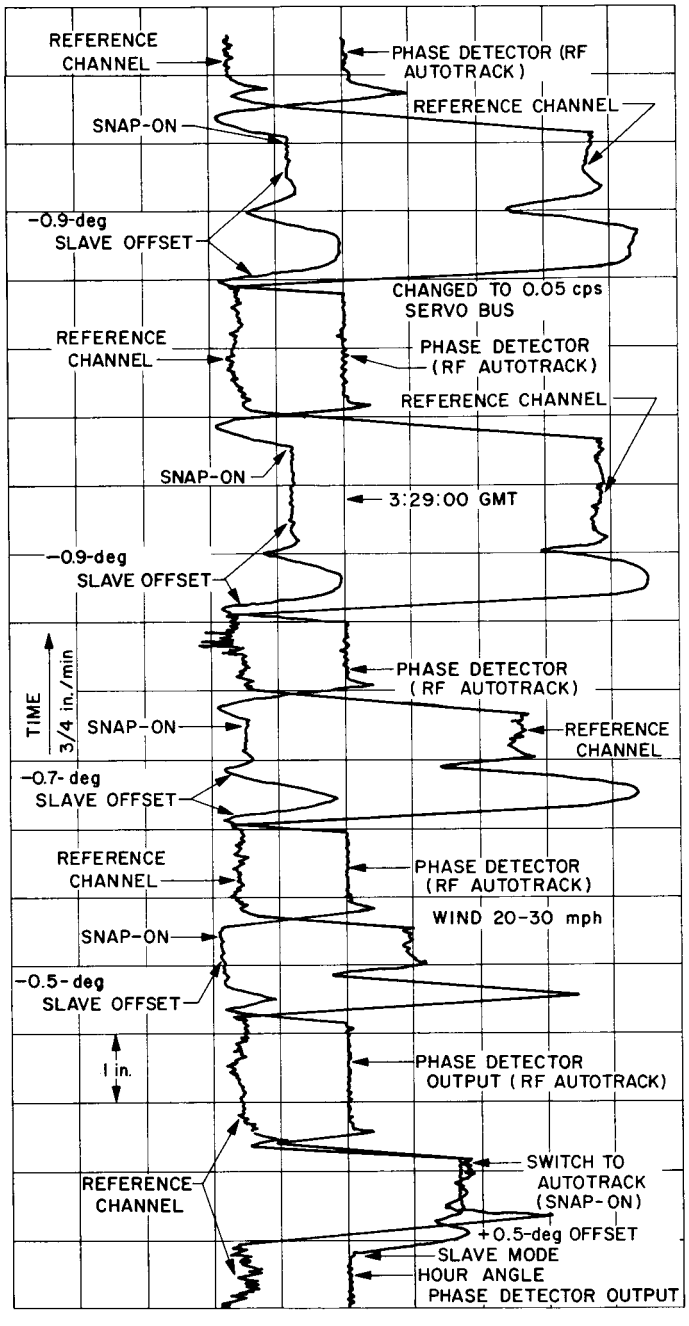


Fig. 9. Snap-on tests on Crab Nebula

where $\delta\theta$ is rms tracking error in radians, λ is wavelength, and D is (circular) aperture diameter in consistent units of length. P_s is source noise power, τ is system time constant, and W is predetection bandwidth. Since P_s and P_n appear only as ratios, we may substitute the temperatures, T_{source} and T_{noise} (T_s and T_n). The effective T_n of this system will be the geometric mean of the two front-end temperatures, approximately 500°K.

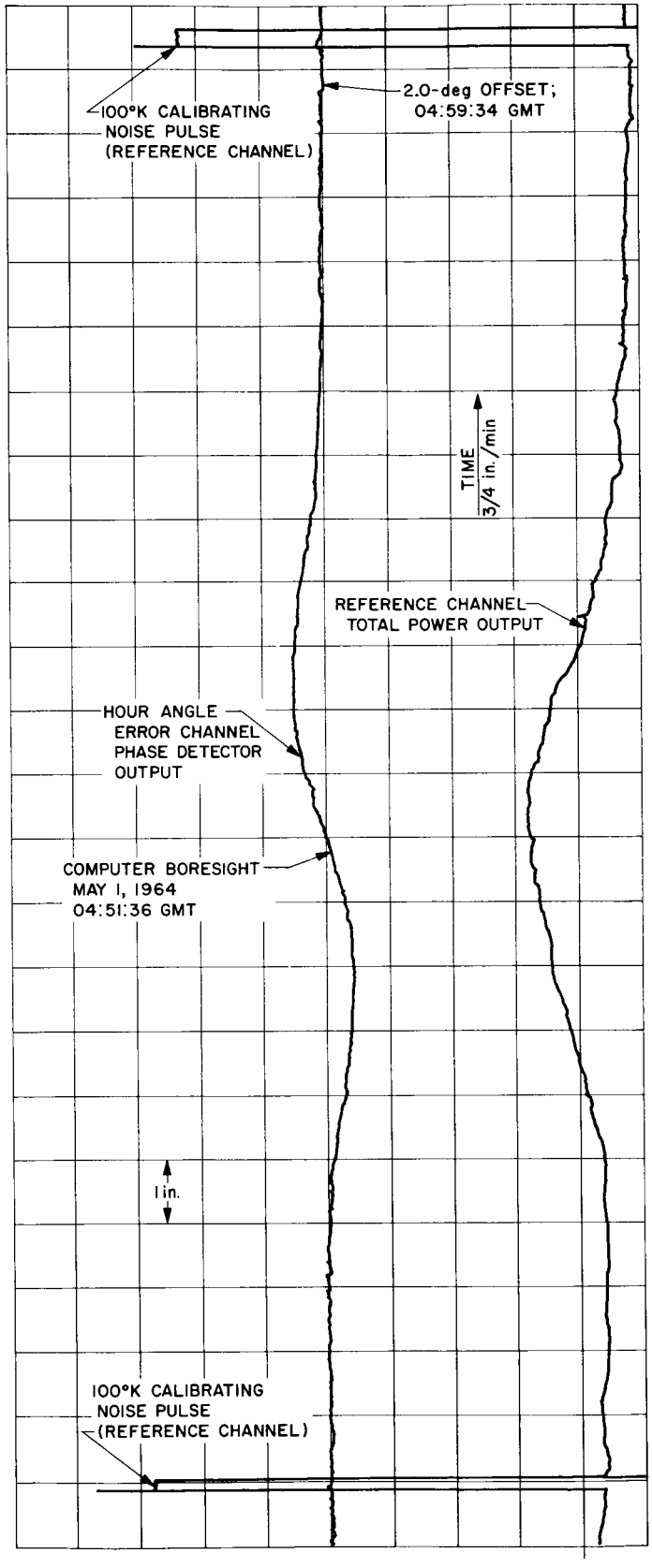


Fig. 10. Drift curve on Virgo A

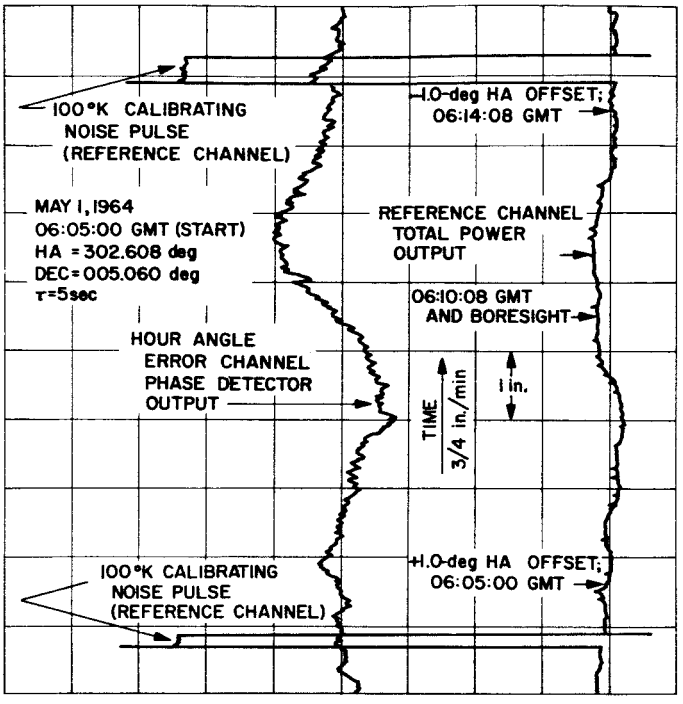


Fig. 11. Drift curve on Hercules A

$$D = 85 \text{ ft}$$

$$\lambda \simeq 1 \text{ ft}$$

$$\frac{P_s}{P_n} = \frac{T_s}{T_n} = \frac{T_s}{500°\text{K}}$$

$$W = 2 \times 10^6 \text{ cps}$$

$$T = 0.1 \text{ sec}$$

For example, Eq. (1) gives an rms error of approximately 0.07 deg for a 5°K source. The values of bandwidth, time constant, and temperature used in the above calculation are very approximate. During the automatic tracking runs, antenna pointing position data were recorded which can be compared with source ephemeris data to derive tracking bias and jitter errors. The results, when available, will be compared with the above approximate analysis.

Refs. 15 and 16 discuss radiometric techniques used to angle-track the Sun for boresight purposes.

4. 1/7-Scale Model Feed for the Advanced Antenna System

Preparations are being made to implement the K_u-band scale model studies of the feed for the 210-ft Advanced Antenna System (AAS). During March and April, work progressed on the Mesa Antenna Range, the 30-ft antenna

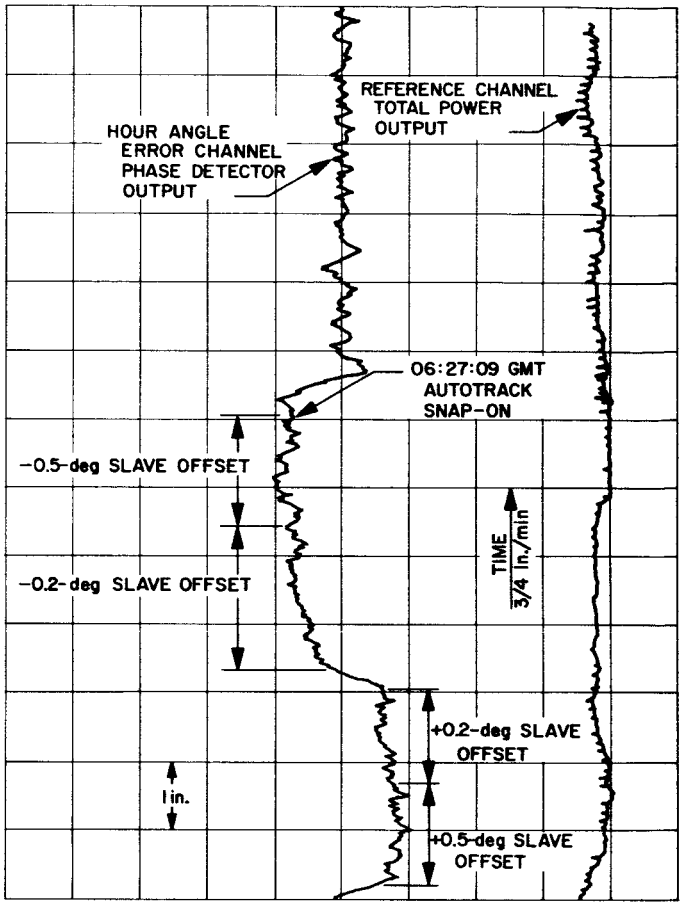


Fig. 12. Snap-on tests on Hercules A

Cassegrain feed cone, the 4-ft-diameter gain standard-illuminator antennas, and the listening and simultaneous lobing model feeds.

The Mesa K_u-band Antenna Range, described in Ref. 17, is 70% complete. This range, which will be used to obtain patterns of the listening and monopulse AAS scale model feeds, is being fitted with a medium duty pedestal to support the horn-subreflector Cassegrain assemblies. The listening feed, a dual mode conical horn of circular cross-section has been fabricated. The monopulse feed, consisting of a linearly polarized bridge and a single multi-mode conical horn of rectangular cross-section, is 20% complete. Fabrication is complete on the scaled subreflector and beam-shaping flange.

Work on the 30-ft antenna Cassegrain feed cone for the model feeds, and work on the 4-ft gain standard-illuminator paraboloid reflector antennas is 80% complete. Design work on the remotely controlled subreflector positioner and the scaled quadripod is continuing.

B. Venus Site Experimental Activities

1. Introduction

The Venus site at Goldstone has been used as a field testing laboratory for development of advanced space communication system and component technology applicable to the DSIF. A principal activity at the site is lunar and planetary radar experiments. The radar experiments involve the same devices as a two-way deep space communications link, excepting an active transponder, e.g., big antennas at high frequency, powerful transmitters, low-noise receivers, signal processing techniques economical of signal-to-noise ratio. The experiments involve radio propagation over the portion of the solar system of concern to present and near-future space communications, and they involve long and continuous operation of the equipments used. For these reasons the radar experiments have been found to be an effective device for accomplishing some of the advanced technology needed to support the DSIF/JPL space communication work. Also, the scientific information obtainable from the radar measurements, e.g., surface characteristics of the Moon and planets and improved determination of their motions and locations, is useful in communications and tracking.

Past issues of the *SPS* (from No. *37-16*, July 31, 1962) have reported the analysis design and building of the equipment for the Venus site and some of the results obtained in the experiments; information on the current status of the S-band planetary radar and recent experiments conducted with it are contained in this report.

Since early this year, the Venus site has been operating continuously, 24 hr a day, 7 days a wk. Part of the purpose in doing this is to experiment with methods for obtaining more efficient use of facilities of this type with a fixed number of personnel. Also, a more continuous use and observation of the equipment and more continuous measurements of space propagation conditions and planet characteristics are desired.

The present series of radar measurements was begun February 18, 1964; since that time there has been accumulated approximately 230 hr of received signal data from Venus, and approximately 40 hr from the Moon. Measurements of the black body radiation of Venus have been made (approximately 10 hr); also, calibrations have been made of the gain and pointing of the 85-ft antenna using radio astronomical sources. The activities are summarized in Table 1.

Table 1. Summary of Venus site radar system experimental activity (February 18 to April 20)

Activity	Approximate total hr
Primary experiments:	
1. Planetary radar	469[a]
2. Lunar radar	82[a]
Secondary experiments:	
1. Venus thermal radiation	10
2. Radio star tracks	110
Testing, calibration, construction maintenance (scheduled)	432
Down time (due to equipment failure includes unscheduled maintenance)	409
Total hours during period: 24 × 63 days	1512

[a]Because of time-shared diplexed monostatic radar, actual radar data is only one-half of these total radar operation times.

Summary data on the performance of the low-noise receiver system during the report period are presented; the measured strength of the received signal returned from Venus is compared with the nominal calculated strength for the recent measurements.

2. Description of Present Lunar/Planetary Radar System

A functional block diagram of the present Lunar/Planetary radar system is shown in Fig. 13. It is a monostatic time-shared continuous wave (CW) system using an 85-ft antenna for transmitting and receiving on planetary targets. For lunar measurements a separate 6-ft-diameter antenna mounted on the 85-ft antenna quadripod apex is used for receiving. The operating frequency is 2388 Mc.

A 100-kw output CW transmitter is used in three modes of operation: low rate on–off keying, phase modulation, or continuous wave operation. A 1.2-Mw capability 400-cps motor generator provides primary power for the transmitter beam voltage. High-voltage vacuum rectifiers are used to supply the high-voltage dc for the klystron (approximately 32 kv at 8.5 amp). The Cassegrain feed can provide right- or left-hand circular or rotatable linear polarization. The gain of the 85-ft antenna is 54.4 db with a 0.2-db loss in the transmitter waveguide yielding a net antenna gain of 54.2 db.

In the receiving connection, the waveguide losses are 0.1 db; thus, the 85-ft antenna has a net gain of 54.3 db. First amplification of the signal is in a traveling wave

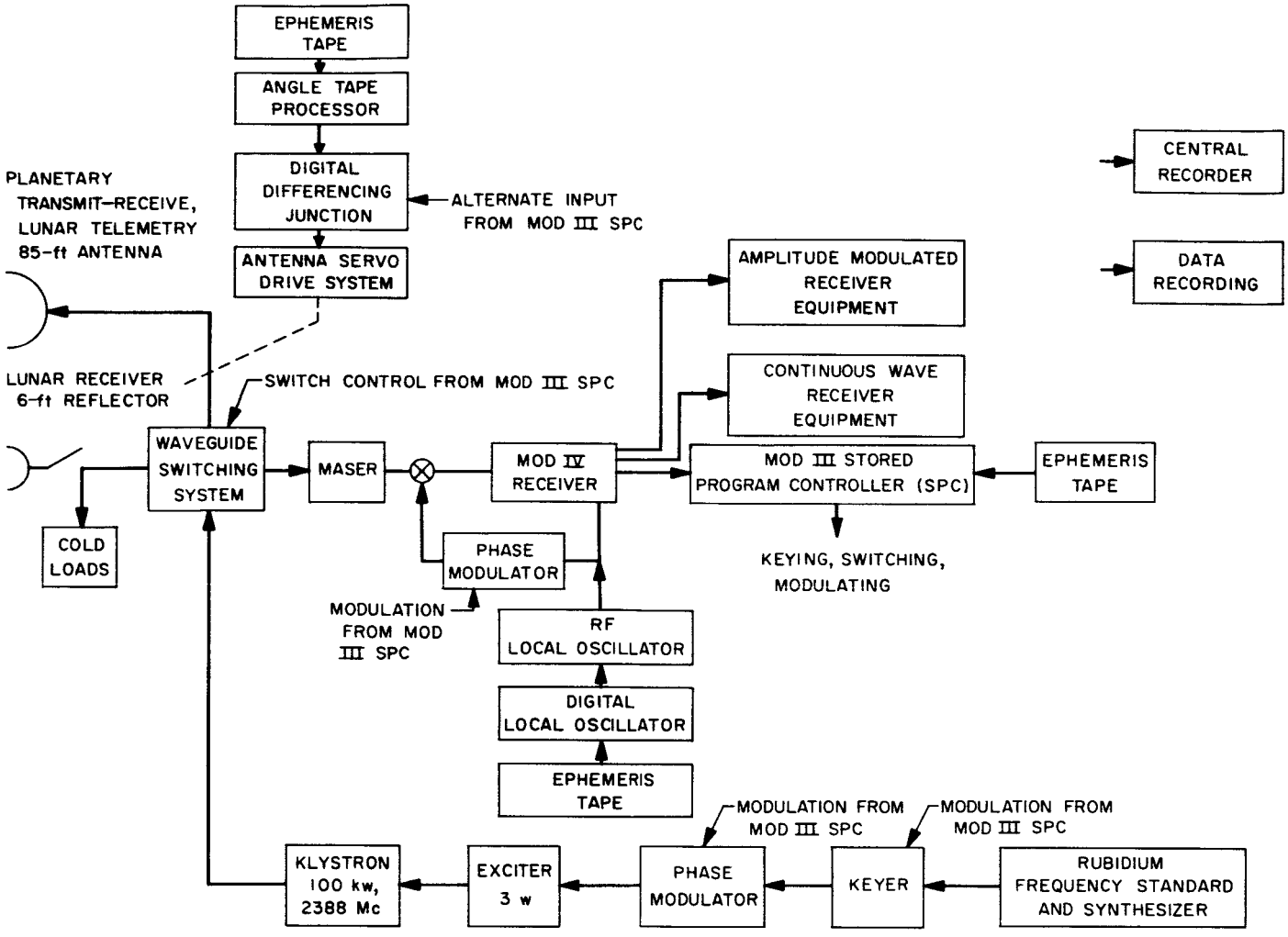


Fig. 13. Lunar/planetary radar basic block diagram

maser using a closed cycle helium refrigerator system operating at approximately 4.4°K. The gain of the maser is approximately 40 db; the total system noise temperature with the antenna at zenith is approximately 29°K. After amplification in the maser the signals are fed to the Mod IV receiver, a multichannel phase-lock loop receiver used to condition the signal for processing and analysis in the amplitude modulated, CW, and ranging terminal equipments. The receiver threshold for synchronous operation in a 10-cps noise bandwidth loop is approximately −176 dbm. When the transmitter is on, the receiver is switched into a nitrogen or a helium cold load; when the receiver is on, the transmitter is switched into an RF water load and the RF drive to the klystron is turned off. All of this RF switching is done by large low-loss waveguide switches which can be manually switched by an operator in the control building or automatically switched by command from the ephemeris controlled Mod III stored program controller equipment. The antenna can be steered by manual control with the aid of a closed-circuit television system with an antenna mounted boresite telescope, or it can be driven in an automatic slave mode from ephemeris data fed into the digital control system.

The Mod III stored program controller (SPC) is used to control the operation of the radar system in both the lunar and planetary modes (Fig. 13). The SPC is supplied with range ephemeris information on punched paper tape for the planetary mode, and with both range and angle ephemeris information for the lunar mode. The time between samples on the planetary range tape has recently been increased from 8 to 60 sec; a linear interpolation is made between sample points. This reduction of sample points has resulted in a considerable saving of time and expense in tape preparation and editing without compromising the accuracy of the range ephemeris.

In lunar and planetary ranging experiments, the SPC is used to control coders which phase-modulate the transmitter and receiver local oscillator. The coder for the lunar mode is a pseudonoise (PN) code generator of length 16,383 with a fixed digit period of 1 μsec. The coder for the planetary mode is a PN code generator of length 511 with a digit period of $125N$, where N may range from 1 to 2^{22} μsec. The planetary mapping experiment (a technique for doing spectral analysis of a range-gated signal) uses the 511 length coders to phase-modulate the transmitter and demodulate the received signal. In all these experiments, the receiver coder is displaced from the transmitter coder by the ephemeris range delay. The SPC programs for the lunar and planetary mapping experiments have been written, debugged, and used in actual experiments. The SPC program for the planetary ranging experiment is being prepared.

In all experiments except the lunar radar, an angle ephemeris paper tape with samples every 64 sec is used to supply information to the angle tape processor (ATP). The ATP supplies information to the digital differencing junction (DDJ) in the same format as that used when information is sent over the microwave link from the coordinate converter computer at the Echo Station. The DDJ compares the ephemeris angles with the antenna position angles and provides an appropriate error signal to control the antenna servosystem. In the lunar radar mode an ephemeris paper tape with samples of range and angles every 64 sec supplies information to the SPC. A buffer has been constructed to allow the SPC to supply the angle information to the DDJ directly in the same format as the ATP and microwave link.

In the planetary amplitude modulation receiver experiment with the single-channel correlator, the SPC is used to modulate the transmitter with a square wave which turns the transmitter on every even second and off every odd second. This technique of synchronizing the keying rate to real time allows the computer to be restarted in the event of power failure without the loss of an entire transmit–receive cycle. The same square wave used to modulate the transmitter is supplied to the single-channel correlator displaced by the ephemeris range delay. The SPC also supplies a transmit–receive signal to the single-channel correlator which automatically stops accumulation at the end of the receive cycle.

In all of the experiments the SPC is used to automatically switch the system from the transmit to the receive mode by means of relays which are program addressable. The length of the transmit or receive cycle is controlled by the range number on the ephemeris tape. A guard delay of 8 sec is used between transmit and receive to allow for mechanical switching of the waveguide switches.

3. Subsystem Performance

a. 100-kw transmitter.

Operation. The transmitter has averaged 12.5 hr of operating time per day during this report period which provided: 634 hr at an average output of 100.6 kw (planetary mode), and 80 hr at 50 kw (lunar mode). The total transmitter filament *on* time was 1140 hr. During this same period of time, the total nonscheduled *off* time attributed to failures of the transmitter system has been 123 hr, the major part of this due to the unavailability of a spare klystron tube. The total time lost due to all other failures of the transmitter and exciter system was about 15 hr.

Modification. The lower ball of the high-voltage crowbar, which houses the firing unit, was replaced with an improved spark plug. The glass insulator used on the earlier unit was unreliable in breaking down the air gap of the crowbar balls and required frequent maintenance (Ref. 18).

New kilowatt (KW) and kilovar (KVAR) meters were installed in the limit-amplifier to provide for better control of the power factor under varying no-load conditions. Due to the large power requirements of the transmitter system it has a considerable interaction with the incoming power supplied to the other Goldstone sites. Also, recording KW and KVAR charts have been obtained so that an accurate continuous record can be kept at the Venus site. These charts and the *Mariner C* high-power transmitter system will be installed this summer.

b. Mod IV radar receiver. During this reporting period the Mod IV receiver has operated in one of five modes continuously without a failure. The modes are: (1) amplitude modulation (AM) receiver using the AM receiver terminal channel with the main receiver local oscillator (LO) controlled by an ephemeris tape programmed VCO; (2) continuous wave (CW) receiver using the CW receiver terminal channel and the main receiver LO controlled as in (1); (3) lunar ranging using the ranging terminal channel and the main receiver LO controlled as in (1); (4) synchronous receiver using the main receiver LO controlled by the VCO in an RF phase-lock loop; and (5) radiometric source tracking using the 30-Mc IF amplifiers in the main receiver to feed a total power detector and data recording system. Routine maintenance has been

performed on the unused channels of the receiver while operating with no need for separate system down time for this work.

The programmed local oscillator system operated within tolerance doppler error (~0.25 cps at S-band) until the last month when erratic doppler errors started to appear. These errors were caused by noisy output from the main 31.44-Mc VCO; the cause of the noise was traced to the source that provides the voltage for the VCO input. The defective modules were replaced and the erratic doppler errors have disappeared.

c. Traveling wave maser. The TWM and closed cycle helium refrigerator subsystem is a prototype of, and basically identical with, the TWM subsystems being developed for the DSIF S-band implementation project. During this period the maser subsystem has been operated for approximately 1400 hr. Fig. 14 is a record of the measured maser gain, and the system noise temperature on the antenna at zenith and on the liquid nitrogen and liquid helium cooled loads. The system temperature shows an increase from 28–30 to 34–36°K over a 20–30 day period. This behavior was not observed in the use of this TWM during the radar experiments last fall. It is suspected that ice formation is the cause since the performance appears to return to normal after the maser is warmed up; this behavior is still under investigation. The approximate 2-db increase in gain which occurs on April 16 and thereafter is a result of recalibration of the gain measurement system cables.

On March 2, the high-voltage power supply for the Vacion vacuum pump kicked off due to overload, causing the maser to become warm. Investigation revealed a leak in the maser input and output ⅞-in. waveguide transitions. New Teflon spacers were cut, grooved, and O-rings added and installed in the maser. This modification resulted in the best vacuum obtained since the installation of the TWM at the Venus site.

On March 20, the maser was shut down for a normal 1000-hr maintenance which includes inspection of the high-speed reduction gears in the crosshead and replacing them if excessive wear has developed. Also, the valves, O-rings, and seals are replaced as well as most of the small bearings in the crosshead drive mechanism. The crosshead is checked for leaks on a test fixture using dry helium as a pressure medium.

During this maintenance period it was decided to modify the crosshead drive from a square wave drive to a sine wave to improve the reliability and wear characteristics by reducing the strain on the gears. This modification was also being considered for the S-band implementation units. The crosshead was modified for sine wave drive at the Echo Station machine shop, reassembled, bench tested, and reinstalled. A normal cool-down procedure was started, but after 3 hr of operation a main start relay (K1 on the CCR compressor) kicked out due to contact failure. The relay was jumpered to make the compressor operational and the maser was then cooled down.

The system was operated in this condition for the next 5 days until a new relay could be installed at a time period that would not interfere with the radar experiments. A spare closed-circuit TV camera with a wide-angle lens was installed to monitor all of the compressor instrumentation in order to ensure safe operation while the interlock circuits were jumpered.

Also, during this time it was necessary to decrease the setting of the J-T valve flow to a setting of 0.006. The original setting had been in the range of 0.017 to 0.0175 in order to maintain a vapor pressure of 17.5, which indicates that the maser is operating at about 4.45°K bath temperature. These readings indicated there might be a failure of the maser due to a restriction in the J-T valve plumbing. Therefore, from April 3 to 8, when the radar system was shut down for other repairs, all lines were carefully vacuum pumped for an extended period to clear out any accumulation of oil or other foreign matter. This resulted in improved cooling capacity of the CCR and a slightly lower bath temperature at normal operation. There was a slight (~1 db) increase in nominal gain of the maser after restart on April 10 (Fig. 14), which is believed to be a result of the slightly lower bath temperature. Also, at this time, the crosshead motor was replaced with a slow speed (72 rpm) Slo-Syn synchronous motor. This crosshead drive system eliminates all of the troublesome gearing; it is being evaluated for use in the DSIF S-band implementation units. So far, operation with it has been completely satisfactory.

The main compressor for the CCR now has approximately 8000 hr operating time on it. The only malfunction that prevented normal operation during this period was due to the vacuum leak which occurred on March 2. All other troubles were worked on with the system in operation.

d. Antenna servo subsystem. The hydraulic system for the 85-ft Az-El antenna was operated without failures during the report period. Normal maintenance and lubri-

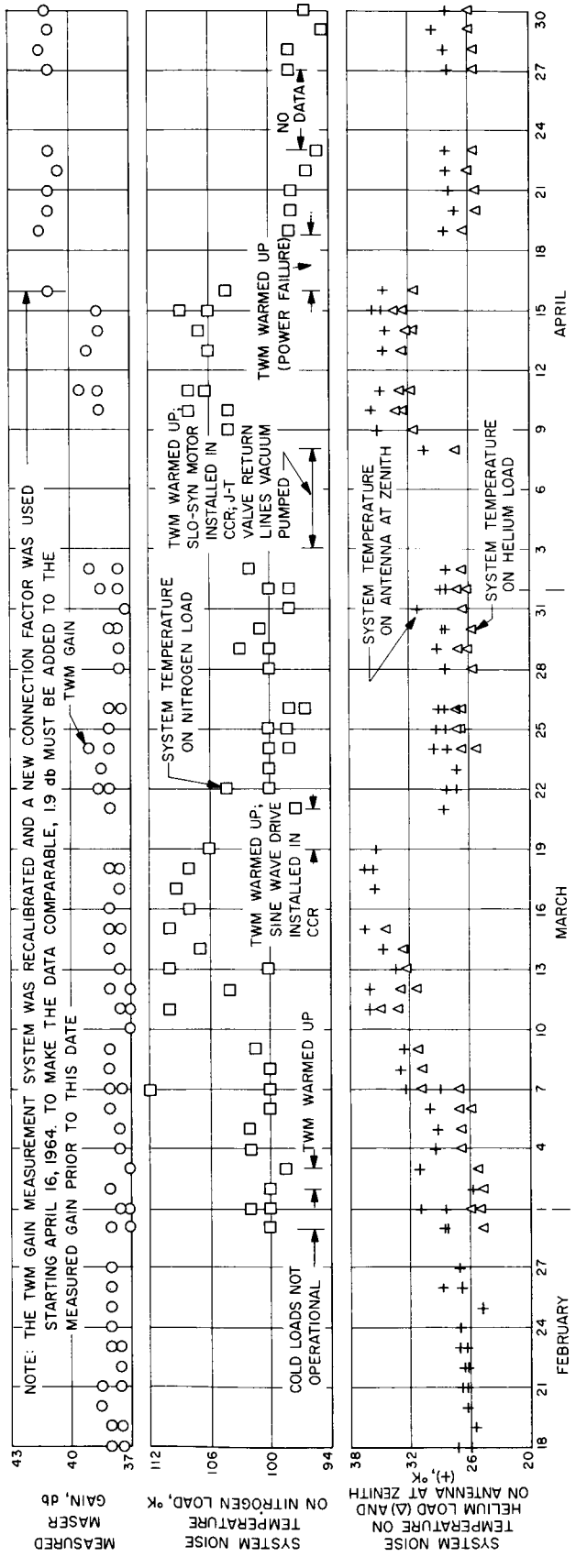


Fig. 14. Planetary radar receiver system temperature and maser gain versus time

cation of the mechanical equipment was accomplished during unscheduled down time resulting from failures elsewhere in the radar system.

Shortly after this tracking period began, the clutch plates in the elevation drive appeared to be slipping while tracking under moderately high wind conditions. The clutch was cleaned and adjusted and appeared to operate in a normal manner until the following morning when the antenna slipped to the final limit from the zenith position. Visual inspection of the clutch plates is not possible because of the physical location of the clutch. It was suspected that the plates were worn to a point where they could no longer be adjusted and would have to be replaced. However, because of the 1 or 2 days out-of-service time required to change the clutch, the clutch plates were locked together and the work held until the next shutdown period when it could be done on a non-interference basis.

The hydraulic low–high speed switching circuit also was disabled so the antenna could not be operated in the high-speed mode. The antenna was operated in this condition, with only low-speed elevation drive available, for approximately 2 wk. During this time a later model clutch was purchased and on March 19 it was installed and a circuit modification made so that it would be compatible electrically. Also, the elevation low-speed tachometer was replaced because of a bearing failure. The new clutch has operated satisfactorily since installation.

Two electronic failures occurred during this tracking period. Four regulator tubes in the elevation electronics +300-v power supply failed. Also, the azimuth high-speed valve driver would not balance because of a tube failure.

The elevation amplifier was reworked because of difficulty encountered in balancing the slave preamplifier. This rework consisted of replacing a potentiometer and reducing the gain of the slave preamplifier.

Approximately 10 hr of tracking were lost due to servo electronics and mechanical failures during the reporting period.

e. Digital equipment. Several new pieces of digital equipment have been added to the Venus site since the last reporting period. An auxiliary rack containing several pieces of input–output equipment and planetary coders has been added to complement the operation of the Mod III SPC. A nine-channel correlator has been connected to the PB-250 to give increased capability in range-gated spectrum analysis. It can provide, essentially in real time, a simultaneous spectrum presentation of the signal within nine consecutive range gates of selectable width. An SDS 910 computer with associated input–output rack has been installed. It will be used initially for slave steering the 30-ft antenna; it has been used experimentally to steer the 85-ft antenna.

Installation of the auxiliary rack and planetary coders on the SPC was rapid because of a new procedure for modifying equipment already installed at the Venus site. The rack and coders were built and checked out on the Mod II SPC at the Pasadena Laboratory. A diagnostic program which checked out both pieces of equipment was then written. The rack and coders were removed from the Mod II, shipped to Goldstone and installed with the Mod III. Cables were already cut to length and could be tied immediately into the input–output patch panel. The diagnostic programs were then used; two logic modules which had been damaged in shipment were located and replaced. No tracking time was lost during the installation and checkout of these two pieces of equipment, an important improvement over previous experience.

A regular maintenance schedule has been established for the Mod III SPC. Individual clocks in each block and each sonic delay line in the machine are checked for timing and adjusted if necessary every 2 wk. When the SPC is not in actual use in the radar system, diagnostic programs are used to check the operation of the machine.

An extensive program of rerouting cables and grounding leads in the SPC has resulted in an increased immunity to electrical noise. Some of the sonic delay lines in the SPC were found to add or delete bits when certain patterns were stored in the lines. A study is now being made of the causes of this problem.

The computer group at JPL has a program which will make polynomial fits to the range, angle, and doppler ephemeris. A program is now being written for the SPC which will allow the computation of the ephemeris from these polynomials. This technique will result in a saving of time and expense in the preparation of punched paper ephemerides tapes.

The operation of all digital equipment has been satisfactory, although occasional power failures result in loss

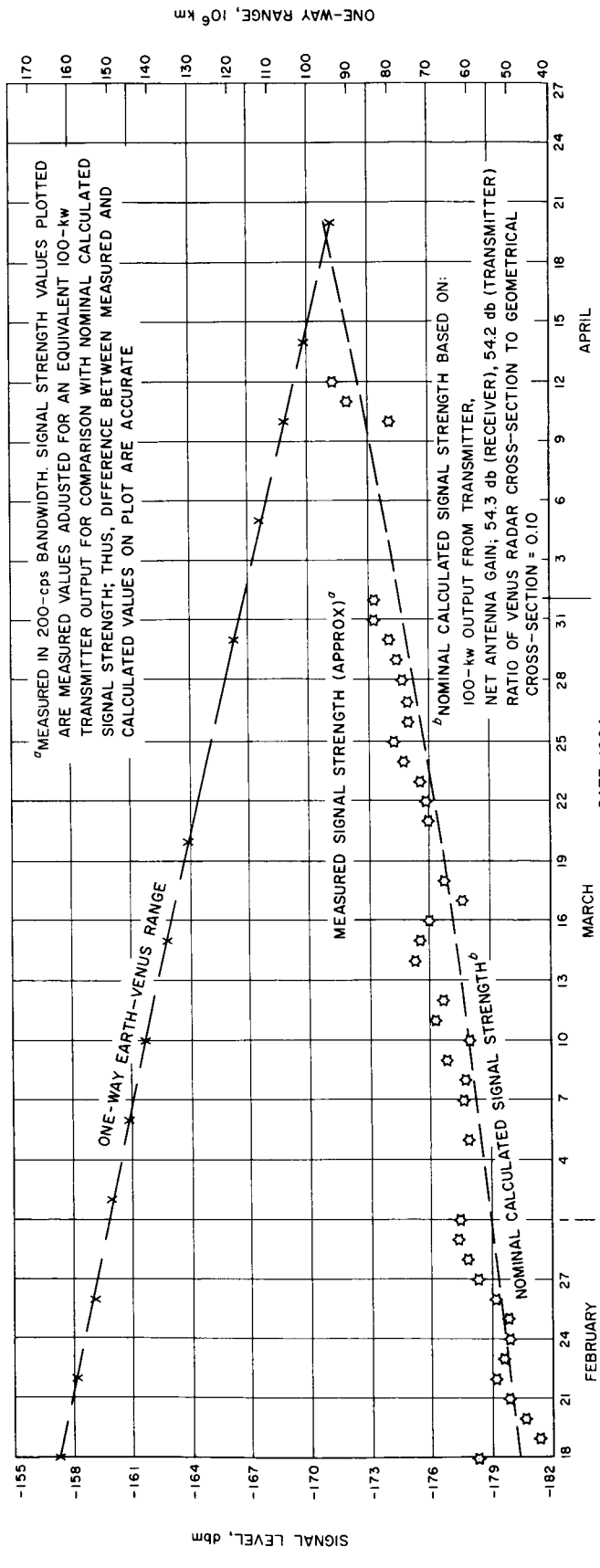


Fig. 15. Comparison between measured and calculated signal strength for Venus radar experiment; range to Venus versus time

of memory on both the PB-250 and SPC because both use sonic delay line memories.

f. Experiments. The experiments performed at the Venus site include: AM signal spectrum and power, CW signal spectrum, range-gated signal spectrum (mapping), phase-lock receiver doppler velocity on the planet Venus, and lunar ranging. All are active radar experiments. The system was also used in a passive mode as a radiometer to make black-body temperature measurements of Venus, and radio star tracks to establish antenna gain, system temperatures, antenna boresight, and servo pointing accuracies.

The AM spectrum experiment uses the single-channel correlator and the PB-250 computer to measure the spectrum and signal strength from the planet Venus. The system temperature is measured during each receive cycle to calibrate the signal strength measurement. Fig. 15 is a plot of the comparison between the nominal calculated and the measured signal strength of the radar signal received from Venus during the present report period. The approximate one-way range to Venus is also shown.

The mapping experiment uses the nine-channel correlator and PB-250 to measure the spectrum and signal strength in nine adjacent range gates. The depth of each range gate is approximately $11.5N$ mi, where N may be any integer. At the conclusion of each receive cycle the nine spectra can be displayed on a Moseley X-Y recorder. The nine signal strengths are typed out by the PB-250.

The CW spectrum experiment records the receiver output after going through a filter and analog-to-digital converter on the magnetic tape of the central recorder. The magnetic tape is sent to Pasadena where the spectrum analysis is made on an IBM 7094 computer.

The phase-lock receiver experiment provides measurement of RF phase-coherent doppler velocity by using the phase-lock loop of the Mod IV receiver rather than the programmed local oscillator. The actual frequency of the phase-locked LO and also the difference between the programmed LO are recorded on the teletype data system.

The lunar ranging experiment uses the Mod III SPC to control the system and process the incoming data. Output of the SPC is a punched paper tape and a number printout showing received signal and noise strength versus the position of the range gate. A graphical presentation of the signal versus range is made in real time on a Moseley X-Y recorder.

C. Planetary Radar Project

1. High-Power 100-kw S-Band Transmitter

a. Introduction. This reporting period has been noted for the extensive mission schedule maintained by the Venus transmitter. System operation was conducted on a three-shift basis with the actual transmitter operation extending up to 18 hr a day on a daily basis. The limited off-time attributed to the transmitter was caused by continuing klystron problems. There were very few transmitter system problems. Late in April there was a failure of another klystron. The tube is being replaced with one having new design features which should prevent a repetition of this failure. The down time caused by klystron failures has been used to install a recently manufactured control cabinet in the high-voltage power supply. A new klystron filament supply, designed in the laboratory, has been installed and tested in the klystron compartment and a study has been undertaken to provide for lifting and installation of the recently arrived solid-state high-voltage rectifier.

b. Silicon rectifiers. A 55-kv solid-state rectifier, capable of furnishing 1 Mw of power, has recently been completed and shipped to the Venus site for use with the 100-kv transmitter. This unit is to be a replacement for the high-vacuum tube-type rectifier presently in use (Ref. 19). It is an oil-immersed assembly with an integral oil–water heat exchanger.

The design is proceeding in order to provide mounting and overhead lifting facilities for the rectifier stacks and tank housing. This will ensure fast and efficient installation and servicing of the rectifier system (Fig. 16). Instal-

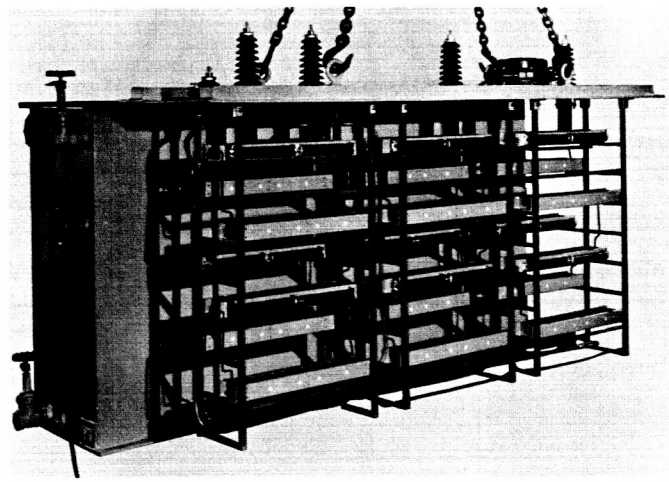


Fig. 16. Solid-state rectifier and tank assembly

lation will be during the next available down time and before the *Mariner C* operational date.

Addition of the solid-state high-voltage rectifier should improve the reliability of the transmitter. The design and operating experience gained from this system will be of great assistance in planning future systems where high-voltage direct current with high reliability is required.

c. DC output cubicle junction box. A new dc output cubicle junction box has been built by the Laboratory and installed in the dc output cubicle of the 55,000-v power supply (Fig. 17). This unit replaces the original subcontracted one which served as the control and junction point for all equipment in the dc output cubicle. The new unit will ensure efficient servicing and greater reliability through the elimination of makeshift wiring and relays exposed to mechanical breakage.

d. Laboratory-designed klystron filament supply. A filament supply for the power klystron, designed and built as an in-house unit, has been installed in the antenna klystron housing (Fig. 18). This unit was designed to replace the original subcontracted power supply which suffered from transformer and filter-choke high-voltage breakdowns as well as failures due to an inadequate rectifier assembly. The new system consists of an oil-filled filament transformer, a corona-shielded rectifier assembly and a corona-shielded filter-choke assembly (Ref. 20).

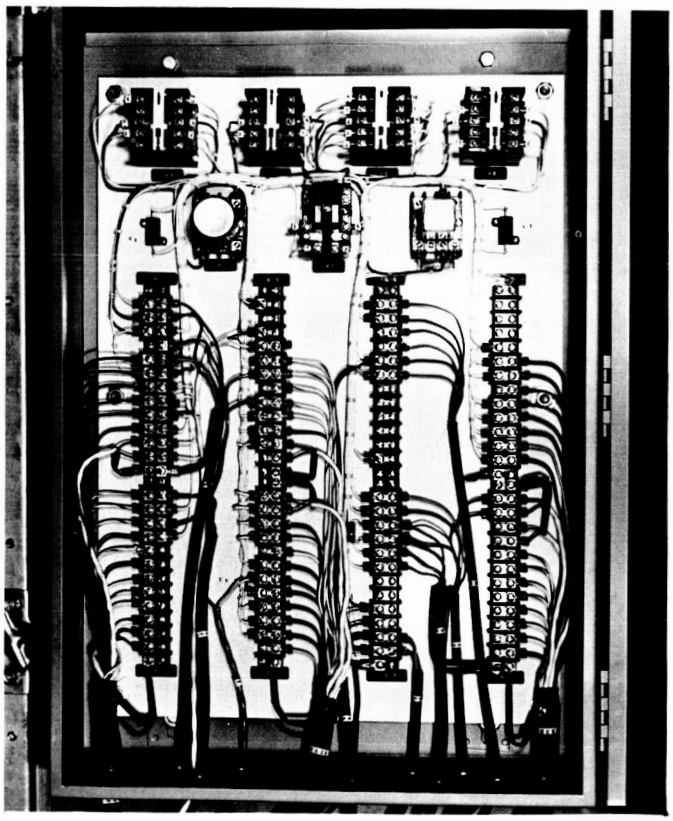


Fig. 17. DC output junction box

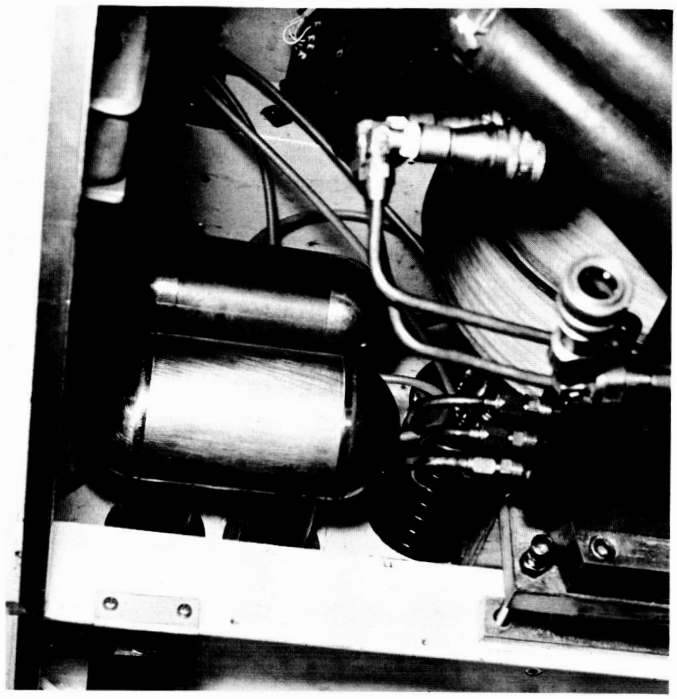


Fig. 18. Klystron filament supply installed

The new filament supply has been operated for 104 hr and has performed perfectly. It has been subjected to klystron degassing crowbars, 300% momentary overload currents, and klystron cathode-to-ground high-voltage arcs without failure, thus proving the reliability and overload protection of the design.

2. Planetary Ranging Coder Subsystem

a. Introduction. A subsystem of planetary ranging coders has been designed and constructed for installation into the Mod III ranging equipment (Ref. 21) at Goldstone. The function of this subsystem is to extend the capability of the Mod III to include planetary ranging experiments. This article is a description of the coder subsystem itself; future articles will describe the use of these coders in planetary ranging experiments.

A block diagram of the coder subsystem is shown in Fig. 19. The various blocks have been grouped into four major units: transmitter coder, receiver coder, range rate number controlled oscillator, and counter. Each unit will

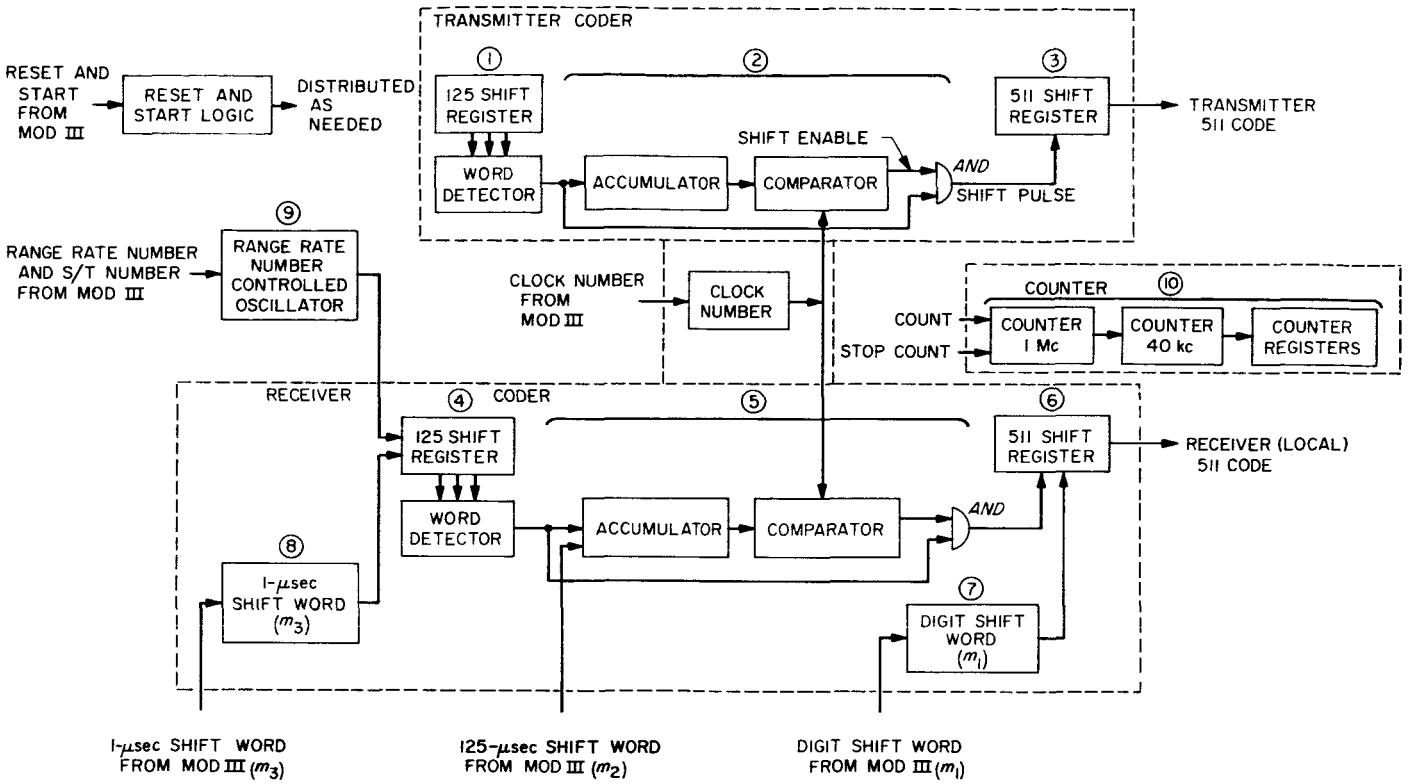


Fig. 19. Planetary ranging coder subsystem block diagram

be described in some detail here. Basically, however, the coder subsystem provides two identical pseudonoise (PN) code signals. One of these is used to modulate a transmitted carrier, and the other is used as a local signal in the receiver for correlation detection of the received signal.

b. Transmitter coder. The transmitter coder consists of the blocks numbered ①, ②, and ③ in Fig. 19. It provides a signal for modulation of the transmitted carrier.

The transmitter code is produced from a maximal length shift register sequence of period 511 digits. The code is produced by assigning a unit of time, called one digit period, to each digit of the period 511 sequence. The sequence is generated by a nine-stage shift register (Block ③) whose input is the Modulo 2 sum of the outputs from Stages 5 and 9 of the register. The state of the shift register at any time, t, is described by a nine-component vector whose components are the outputs of the various stages at time t. For example, the ith component at time t is the output of the ith stage of the shift register at time t. The shift register changes state each time a shift pulse occurs, so that the length of a digit period is equal to the interval of time between successive shift pulses.

The output of Stage 6 of the shift register is tapped to provide the transmitter code, and the digits of the code appear sequentially in time at the rate of 1 digit per shift pulse. Since the shift register sequence has period 511 digits, the length of the code in seconds is given by

$$p_c = 511 \cdot t_d \tag{1}$$

where t_d is the digit period (the length of time between successive shift pulses).

The shift pulses which drive the period 511 shift register are produced by counting down a 1-Mc pulse train. The countdown operation is performed by the Blocks ① and ② of Fig. 19. Block ① consists of a seven-stage shift register and a word detector. The shift register generates a sequence of length 125 at a clock frequency of 1 Mc, so that the shift register changes state once each microsecond. The word detector on the period 125 shift register recognizes one particular state of the register and produces an output each time that particular state occurs, that is, once each 125 μsec. The first stage of the countdown process is, thus, a divide by 125 which yields a nominal 8-kc pulse train from the 1-Mc reference.

Each time a 125-μsec word detector pulse occurs, a +1 is added into the contents of an accumulator, Block ② in Fig. 19. Following each addition, the content of the accumulator is compared with a constant number, called the clock number. If the content of the accumulator is less than the clock number, the accumulator waits for the next addition to occur. If the content of the accumulator is greater than, or equal to, the clock number, an enable signal is activated and the clock number is subtracted from the content of the accumulator. The next 125-μsec pulse to occur after the enable signal has been activated performs two functions: it causes a +1 to be added into the accumulator, and the combination of the enable signal and the 125-μsec pulse produces a shift pulse to the period 511 shift register. The enable signal then turns off, and the process of adding +1's into the accumulator continues until the accumulator sum once again becomes equal to the clock number. It follows that the time interval between successive shift pulses is given by

$$t_d = N_{cl} \cdot 125\ \mu\text{sec} \tag{2}$$

where N_{cl} denotes the clock number. Thus, the second stage of the countdown process yields a pulse train whose nominal frequency is $8 \cdot 10^3 \cdot (N_{cl})^{-1}$ cps.

Combining Eqs. (1) and (2) gives

$$p_c = 511 \cdot 125 \cdot N_{cl}\ \mu\text{sec} \tag{3}$$

as the length of the transmitter code in μsec. The clock number, N_{cl}, may be any (nonzero) positive integer depending upon the digit period desired. The value of N_{cl} is inserted from the Mod III into a storage register in the coder subsystem prior to the start of a ranging experiment.

c. Receiver coder. The receiver coder, Blocks ④–⑧ in Fig. 19, is similar to the transmitter coder. In fact, Blocks ④, ⑤, and ⑥ are essentially identical to Blocks ①, ②, and ③, respectively, in the transmitter coder. Such differences as do exist arise from the fact that the receiver coder, which produces a local signal for use in correlation detection, must be capable of being shifted in phase relative to the transmitter coder, so that the local signal may be matched in phase to a received radar echo.

Unit code shifts. Shifting the local code amounts to deleting or repeating digits or a fraction of a digit in the receiver period 511 shift register. Shifts are accomplished by varying the rate at which shift pulses appear to drive the period 511 shift register.

There are three different unit shifts available for use in bringing the local code into phase with a received signal. These shifts are of different magnitudes and may be used singly, or in combination. The unit shifts available are: ± 1 μsec, -125 μsec, and $\pm t_d$ μsec where a plus (+) shift refers to a delay of the local signal (right shift) and a minus (−) refers to an advance of the local signal (left shift) in phase relative to a fixed reference. A single unit shift of +1 μsec (−1 μsec) causes the local code to delay (advance) in phase by 1 μsec relative to a fixed reference. A single unit shift of −125 μsec causes the local code to advance in phase by 125 μsec. (There is no provision for a right shift in this unit.) A single unit shift of $+t_d$ μsec ($-t_d$ μsec) causes the local code to delay (advance) in phase by one full digit period, that is, $N_{cl} \cdot 125$ μsec.

Implementation of unit code shifts. A unit shift of +1 μsec is accomplished by lengthening one period of the period 125 shift register by +1 μsec. Normally, this register cycles through 125 states during each 125-μsec interval. If, however, during the course of one cycle the register is made to repeat one of the states in the cycle, that particular cycle will be 126 μsec long. The state which produces the word detector output will be 1 μsec late during the shifted cycle, and thus all subsequent word detector pulses will be delayed by 1 μsec relative to a nonshifted reference. Suppose that the first comparison between the accumulator and the clock number to pay off following the 1-μsec shift has occurred, so that the enable signal is activated. The next 125-μsec pulse to occur will produce a shift pulse to the period 511 shift register, but, of course, this 125-μsec pulse occurs 1 μsec late relative to a nonshifted reference. The effect of the 1-μsec delay in the shift pulse is that some digit in the local code is lengthened by 1 μsec, thus causing a delay of 1 μsec in the local code.

A unit shift of −1 μsec is accomplished by shortening one period of the period 125 shift register by 1 μsec. In this case, the register is made to skip one of the states in the cycle, so that the shifted cycle is 124 μsec long. The word detector output occurs 1 μsec early during the shifted cycle, and thus all subsequent word detector pulses occur 1 μsec early relative to a nonshifted reference. Finally, the next shift pulse to the period 511 shift register occurs 1 μsec early, thus shortening some digit in the local code and advancing the code by 1 μsec.

The state which is either repeated or deleted to produce shifts in the unit ± 1 μsec is the all 1's state. Details concerning the technique for mechanizing this unit shift are given in Ref. 22.

A unit shift of -125 μsec is accomplished by adding an additional $+1$ into the 125-μsec word detector accumulator. Normally, the content of this accumulator increases by $+1$ each time a 125-μsec word detector pulse occurs until the number in the accumulator is equal to the clock number. If an additional $+1$ is inserted into the accumulator during one of the countup cycles, the sum in the accumulator will become equal to the clock number 125 μsec early, the shift pulse enable will become activated 125 μsec early and, thus, the next shift pulse to the period 511 shift register will occur one 125-μsec pulse early. The net effect is that some digit in the local code will be shortened by 125 μsec and the code advanced by an equivalent amount relative to a nonshifted reference.

A unit shift of -1 digit period is accomplished by inserting an additional shift pulse between two normally occurring shift pulses to the period 511 shift register. The additional shift pulse immediately advances the period 511 shift register to the next state, so that when the next normally occurring shift pulse appears, the local code has been advanced in phase by one digit relative to a nonshifted reference.

A unit shift of $+1$ digit period is more involved and requires a short digression. Clearly, a unit digit period shift to the right could be accomplished by deleting one of the normally occurring shift pulses. The period 511 shift register would then remain in some one of its states for two consecutive digit periods, so that when normal shifting resumed the local code would have dropped one digit behind a nonshifted reference. This method, however, would be undesirably slow in the case where the number of digits to be shifted is large and the digit period is long. For example, 100 digit shifts to the right with a digit period of 1 msec would require 0.1 sec for completion.

In the planetary coder subsystem, an alternative method is employed which permits digit shifts to the right to occur as rapidly as digit shifts to the left. A digit shift to the right is accomplished by making the period 511 shift register "back up" one state during the interval between two normally occurring shift pulses. Let $n-1$ and n denote two consecutive shift pulses to the period 511 shift register occurring at times $t = n-1$ and $t = n$, respectively. Let $n-1$ cause the period 511 shift register to advance from state S_{n-1} to state S_n, and n cause the transition $S_n \rightarrow S_{n+1}$ to occur. Now, if the shift register is made to back up one state between the shift pulses $n-1$ and n, then both $n-1$ and n will cause the transition $S_{n-1} \rightarrow S_n$, so that the shift register will drop one state behind a nonshifted reference or, equivalently, the local code will be delayed (shifted right) by one digit.

Fig. 20(a) is a block diagram of a period 511 shift register with only the normal shift logic present. The input to every stage of the register except the first stage is the output of the preceding stage of the register. The input to the first stage is the Modulo 2 sum of the outputs of Stages 5 and 9. When a shift pulse occurs, a new digit appears at the output of the first stage, and all other digits in the shift register move one stage to the right. Fig. 20(b) shows the same period 511 shift register with only the back-up logic present. In this case, the input to each stage of the register except the last stage is the output of the succeeding stage. Thus, when a back-up pulse occurs, the digits in the shift register move one stage to the left. It is interesting to note that the input to the last stage of the register is formed by the Modulo 2 sum of the outputs of Stages 1 and 6.

Fig. 21 illustrates the processes of shifting right and left in the unit of one digit. Waveform *a* denotes a succession of shift pulses to a period 511 shift register. Waveform *b* is a portion of a code output from a reference shift register. A new digit is produced following each shift pulse, corresponding to a change of state of the register. Waveform *c* is a portion of a code output from a shift register which is synchronous with the reference at time $t = 0$. Partly through Digit 6, a shift-right pulse occurs which causes the register to back up one state and the code output to revert to its previous value. The net effect of the shift-right pulse is to delay the output by one full digit as can be seen by comparing the relative positions of Digits 7 on with the corresponding digits in the fixed reference. In waveform *d* a shift-left pulse occurs part of the way through Digit 6 which causes the register to advance one state and the code to shift left by one digit relative to the reference.

Utilization of unit code shifts. The unit code shifts are used to bring the local code into phase with a received signal. Suppose that the received signal and the local code are stationary in phase with respect to one another, but that the received signal has been delayed by a total of $+L$ μsec, that is, the origin of the received signal is displaced to the right of the origin of the local signal by L μsec. Since the codes are periodic, it is not necessary to shift the local code by integral numbers of complete code periods. In any event, the number of

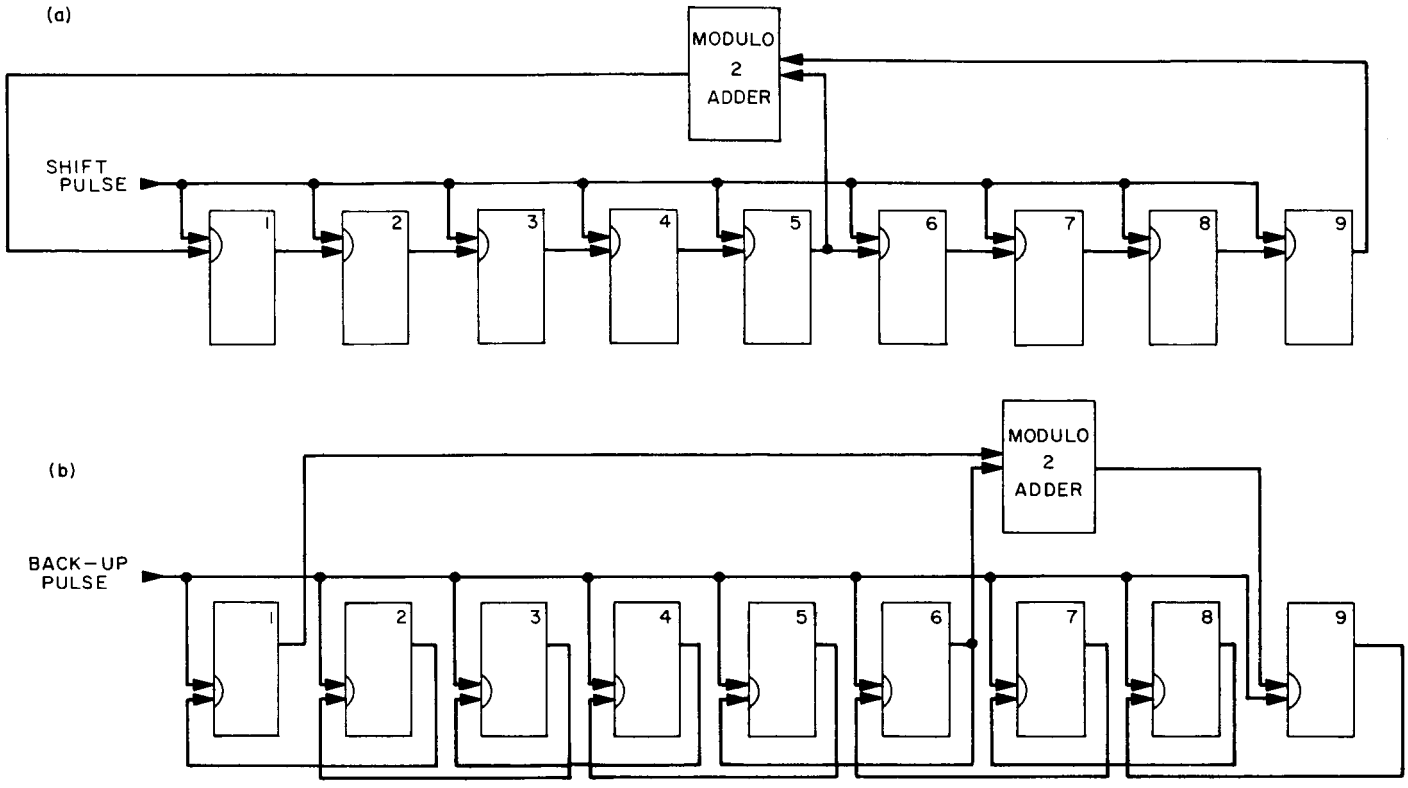


Fig. 20. Period 511 shift register

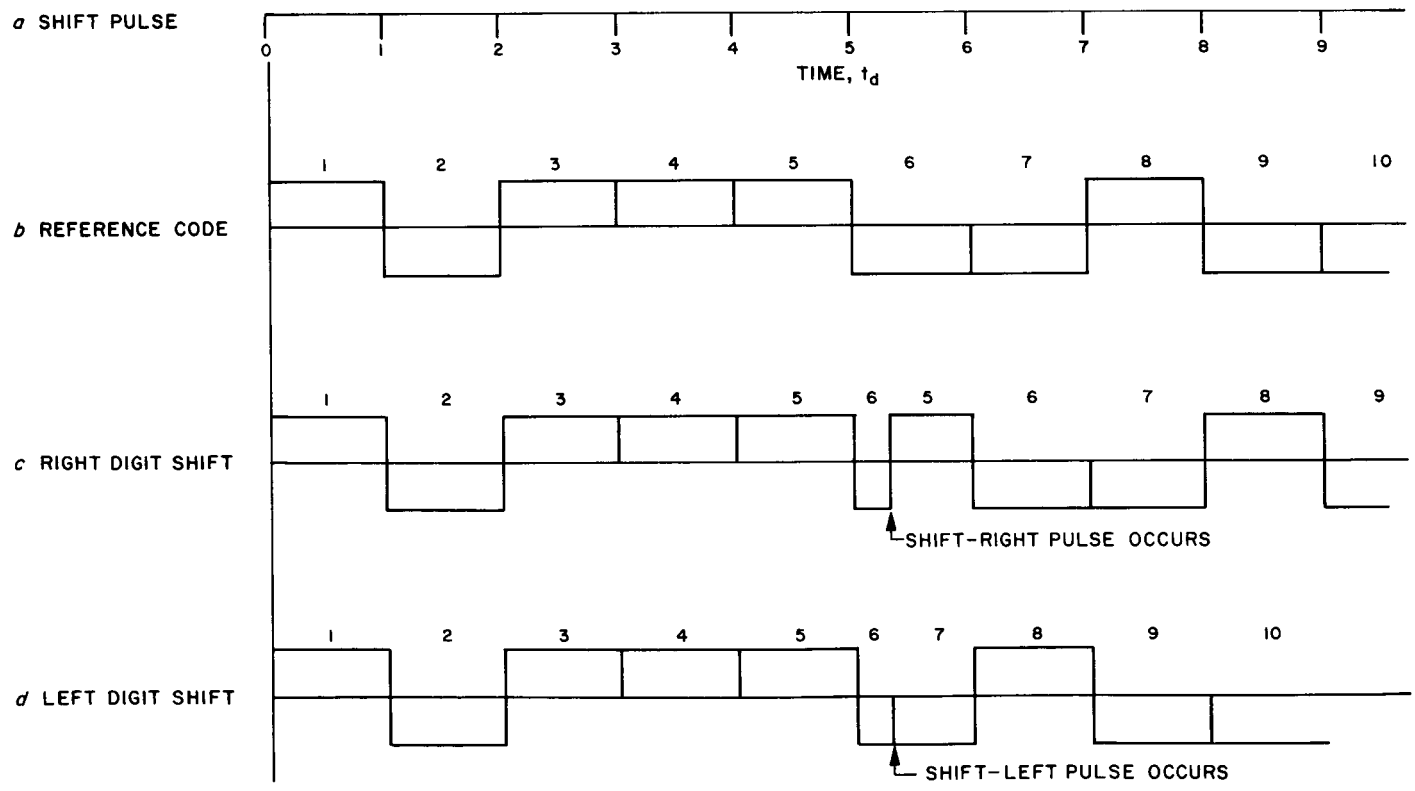


Fig. 21. Left and right digit shifts

microseconds, M, by which the local code must be shifted is given by

$$M = L \text{ (modulo } p_c) \tag{4}$$

where p_c is given by Eq. (3).

Now, the number M may be written as the sum of three components as follows:

$$M = m_1 \cdot (+t_d) + m_2 \cdot (-125) + m_3 \cdot (+1)\ \mu\text{sec} \tag{5}$$

where m_1, m_2, m_3 are integers, and

$$m_3 \leq 124$$

and

$$M - m_1 \cdot (+t_d) < t_d$$

Clearly, the particular factorization expressed in (5) is not unique, since, for example, the factorization

$$M = m_1 \cdot (+t_d) + m_2' \cdot (-125) + m_3' \cdot (-1) \tag{6}$$

where

$$m_2 - m_2' = +1$$

and

$$m_3 + m_3' = 125$$

is also valid. The purpose of the factorization process is to break the number M up into an integral number of unit digit shifts plus an integral number of unit 125-μsec shifts plus an integral number of unit 1-μsec shifts. The particular factorization chosen, however, is at the discretion of the programmer.

The numbers m_1, m_2, and m_3 are inputs to the coder subsystem from the Mod III. For each m_i, the number of unit shifts produced is dependent upon the magnitude only of m_i. The sign of m_i is used to indicate the direction of the shifts, that is, either left or right. For m_1 and m_3, a positive number produces right shifts of the local code and a negative number produces left shifts of the local code. The number m_2 must always satisfy $m_2 \geq 0$, and a positive m_2 produces left shifts of the local code.

The numbers m_1 and m_3 are inserted into storage registers in the coder subsystem, Blocks ⑦ and ⑧, respectively, of Fig. 19, and the number m_2 is added directly into the 125-μsec word detector accumulator in the receiver coder. When m_1 is loaded into its register, additional logic associated with the register starts to produce shift pulses in the unit $\pm t_d$ μsec. Each time a shift pulse is produced, the number in the register is decremented by $+1$ if the number is positive or incremented by $+1$ if the number is negative. When the number in the register reaches zero, the production of shift pulses ceases. An identical procedure applies to the number m_3 except, of course, that the shift pulses produced are in the unit ± 1 μsec. If a second input shift number is added into either the m_1 or the m_3 register while a previously loaded number is being counted down, the net result in the register is the algebraic sum of the new shift number and the register contents at the time that the addition occurs. Thus, it is not necessary to wait for either the m_1 or m_3 register to count down to zero before a new shift word is loaded into the register.

Time requirements for shifting. The time required to complete a total of M shifts is a function of the algorithm used to compute the m_i. Shifts in the unit $\pm t_d$ μsec are performed at the rate of 1 shift per 25 μsec, while shifts in the unit ± 1 μsec are performed at the rate of 1 shift per 125 μsec. Shifts in these two units are accompanied by a countdown process in both the m_1 and m_3 storage registers. Shifts in the unit -125 μsec are not accompanied by a countdown process, since shifting in this unit is synonymous with augmenting the sum in the 125-μsec word detector accumulator. A previous inequality ($M - m_1 \cdot t_d < t_d$) implies that

$$m_2 \cdot 125 < t_d$$

and thus, from (2), it follows that

$$m_2 < N_{cl}$$

That is, the number of 125-μsec shifts to the left is always less than one clock number. In this case, shifts in this unit are completed when the number of desired shifts, m_2, has been added into the 125-μsec word detector accumulator. Neglecting the time required to perform the addition, it follows that shifts in the unit -125 μsec are completed in zero time. In the eventuality that m_2 is made greater than one clock number, shifts in the unit $-t_d$ μsec will be produced at the rate of 1 shift per 25 μsec until the content of the 125-μsec word detector accumulator becomes less than N_{cl} through repeated subtractions of the clock number (one subtraction occurring each time a digit shift occurs).

Shifting in each unit starts as soon as a number has been loaded into the appropriate line. Interlocks in the subsystem interweave shifts produced in the various units to ensure that all of the asked-for shifts are completed. Assuming a worst-case condition, namely, that shifts in the various units are ordered sequentially in time so that all shifts in one unit are completed before shifts in another unit are initiated, the time required to complete M shifts is given by

$$T = [\,|m_1| + 5\,|m_3|\,] \cdot 25\ \mu\text{sec} \tag{7}$$

where the additional assumption has been made that $m_2 < N_{cl}$. For the two algorithms (5) and (6), the shift times are

$$T_5 = (m_1 + 5m_3) \cdot 25\ \mu\text{sec}$$

and

$$T_6 = (m_1 + 5m_3') \cdot 25$$

$$= [m_1 + 5\,(125 - m_3)] \cdot 25\ \mu\text{sec}$$

Then $T_6 < T_5$ if, and only if, $m_3 > 62.5$. The maximum difference, $(T_5 - T_6)_{\max}$, occurs for $m_3' = 1$, whence

$$(T_5 - T_6)_{\max} = 15.5\ \text{msec}$$

An upper bound on the time required to perform M shifts using a combination of all three units may be obtained via the following argument. Clearly, a total of more than 256 unit digit shifts need never be performed since, for example, a shift to the right of 300 digits is equivalent to a left shift of $511 - 300 = 211$ digits. Further, the number of 125-μsec left shifts need never exceed the number of 125-μsec intervals contained in one digit period since otherwise the same shift could be accomplished by some combination of digit shifts plus 125-μsec shifts to the left. Finally, the number of ± 1-μsec shifts need never exceed 125. Thus

$$T < 256 \cdot 25 + 125 \cdot 125 = 22.025\ \text{msec} \tag{8}$$

d. Range rate number controlled oscillator (NCO). Motion of a radar target relative to an Earth-based antenna introduces a rate component into the phase of a received signal relative to the local code. This rate component must be removed before correlation detection of the received signal can occur. The range rate NCO, Block ⑨ in Fig. 19, removes the rate component between the received signal and the local code by shifting the local code continuously in phase at the same rate that the received signal is changing phase.

The NCO accepts as its input a binary number, the rate number, and produces as its output a number of pulses equal to the rate number which are spaced approximately uniformly in time. A new rate number is read into the NCO each ΔT sec. The number read in at, say, time T_1, is the number of 1-μsec shifts which the receiver coder must complete during the next interval of ΔT sec so that at time $T_2 = T_1 + \Delta T$ the local code will be exactly in phase with the received signal. The output pulses produced by the NCO comprise a shift pulse input to the receiver coder in the unit ± 1 μsec. (These shift pulses are distinct from the pulses produced by counting down m_3.) The number of output pulses produced is dependent upon the magnitude of the rate number only. The rate number sign determines the direction of shift of the receiver coder, a positive number producing shifts to the right and a negative number producing shifts to the left.

The NCO consists of three storage registers, called the rate number, the rate accumulator, and the shifts per unit time (S/T) number, and some associated logic (Fig. 22).

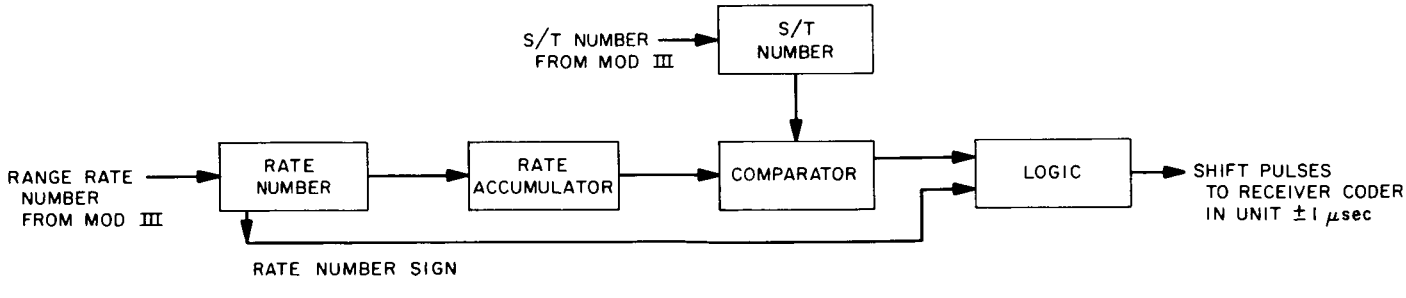


Fig. 22. Range rate number controlled oscillator block diagram

The NCO operates as follows. At the start of each interval of ΔT sec, a new rate number is loaded into the rate number register from the Mod III under program control. The absolute value of the rate number is then added into the rate accumulator at the rate of 40,000 adds per sec during the interval ΔT sec. Following each addition of the rate number, the content of the rate accumulator is compared to a constant number, the S/T number, which has been preloaded into the S/T number register. If the content of the rate accumulator is less than the S/T number, no additional operations occur. However, if the content of the rate accumulator is equal to, or greater than, the S/T number, an output pulse is produced and the value of the S/T number is subtracted from the content of the rate accumulator. (Addition of the rate number every 25 μsec is not affected by these additional operations.) When an interval of ΔT sec ends, the old rate number is erased and a new one inserted into the rate number register. The rate accumulator is zeroed each time a new rate number is inserted into the rate number register.

The range rate numbers are computed by the Mod III ranging equipment from data supplied on a range ephemeris punched paper tape. Successive rate numbers are loaded from the Mod III into the rate number register in the NCO at intervals of ΔT sec. The S/T number, the constant number used for comparison with the rate accumulator, is given by the following expression

$$\text{S/T number} = 40{,}000 \cdot \Delta T \qquad \text{shifts}/\Delta T \text{ sec} \tag{9}$$

with ΔT a positive integer. The S/T number corresponding to a value assumed for ΔT must be inserted into the S/T number register from the Mod III prior to loading a range rate number.

It was stated previously that output pulses from the NCO are spaced approximately uniformly in time. A more precise statement regarding the distribution of output pulses in time is: For a given rate number, say N, loaded at time T_1, the number of output pulses, Q, produced through time $T_1 + t$ sec, $0 \leq t \leq \Delta T$, is given by

$$\begin{aligned} Q(t) &= \text{Int}\left\{\frac{40{,}000 \cdot N \cdot t}{\text{S/T number}}\right\} \\ &= \text{Int}\left\{N \cdot \left(\frac{t}{\Delta T}\right)\right\} \end{aligned} \tag{10}$$

where Int { } denotes the integral part of the expression contained in the brackets. Clearly, $Q(\Delta T) = N$.

Output pulses from the NCO become shift pulses to the receiver coder in the unit ± 1 μsec. These shift pulses are in addition to, and independent of, any shift pulses in the unit ± 1 μsec which may be arising from a countdown of a number m_3. The maximum rate at which shifts can be performed in the receiver coder in the unit ± 1 μsec is 1 shift per 125 μsec, or 8000 shifts per sec. It follows that, in 1 sec,

$$\left\{\begin{array}{c}\text{number of range}\\ \text{rate shifts}\\ \text{completed (right}\\ \text{or left)}\end{array}\right\} + \left\{\begin{array}{c}\text{number of shifts}\\ \text{from } m_3 \text{ count-}\\ \text{down completed}\\ \text{(right or left)}\end{array}\right\} \leq 8000 \tag{11}$$

The interlock circuitry mentioned previously assigns priority to shift pulses arising from the NCO. Thus, if the NCO is producing shift pulses at the rate of 8000 shifts per sec, none of the shifts demanded by m_3 will be completed. This is not to say that the number m_3 will be "lost." In fact, no countdown of m_3 will occur at all in this case. Rather, the number m_3 will remain stored in the m_3 storage register. If, at some later time, the number of shift pulses coming from the NCO falls below the maximum permissible rate, a countdown of m_3 will automatically start.

e. Counter. A counter has been built into the coder subsystem to facilitate checkout of the various shift modes. The counter makes it possible to measure the phase displacement, in units of microseconds, between the transmitter code and the local code. The measurement obtained is accurate to 1 μsec independent of how large or small that displacement may be.

The counter, Block ⑩ in Fig. 19, consists of two counting stages. The first stage counts at 1 Mc and drives a second stage which counts at 40 kc. The counter also includes two storage registers which store the low-order and high-order digits of the counter word. The counter operates in the following manner. A *count* signal from the transmitter coder starts the counter, i.e., the first stage of the counter commences counting a 1-Mc pulse chain. On the occurrence of a 25-μsec clock pulse, the content of the first stage of the counter is added into the second stage while the first stage continues counting. The first stage of the counter is effectively reset during this transfer operation, but the stage never shows all zeroes because it is counting at its maximum rate, and thus a new count is starting even while the old count is being transferred to the second stage. Counting continues in this fashion until a signal from the receiver coder occurs, at which time counting stops and the words

in both of the counter stages "freeze." On the first 25-μsec clock pulse following the *stop count* signal, the content of the first stage is added into the second stage, and then the total count is transferred from the second stage into one or both of the counter storage registers. (The low-order register is sufficient unless the counter word exceeds 2^{25}.) The counting stages then reset and wait for the next *count* signal from the transmitter coder to occur.

The counter may be programmed, via an instruction from the Mod III, to count phase displacement between the transmitter and receiver codes at any one of three points in the two coders. These three points are at the period 511 shift registers, at the outputs of the two 125-μsec word detector accumulators, and at the outputs of the two 125-μsec word detectors. The choice is indicated by pulsing any one of three flip-flops in the Mod III (count 511, count digit, and count 125, respectively). Whenever any one of these three flip-flops is pulsed, the counter resets and waits for the next appropriate *count* signal to occur.

Suppose that the counter is to measure the phase displacement between the two codes at the period 511 shift registers. In this case, the *count* signal from the transmitter coder is the output of a word detector on the transmitter period 511 shift register which recognizes a particular state of the register, and the *stop count* signal from the receiver coder is the output of a word detector which recognizes the same state in the receiver period 511 shift register. The counter thus measures the time interval, in microseconds, between the occurrences of these two word detector outputs. Using the notation of Eq. (5), the counter at this point measures the total displacement M between the two codes, where

$$M = m_1 \cdot t_d + m_2 \cdot 125 + m_3 \ \mu\text{sec}.$$

If the counter is programmed to count at the outputs of the two 125-μsec word detector accumulators, then a *count* signal occurs every time a shift pulse to the transmitter period 511 shift register is produced, and a *stop count* signal occurs each time a shift pulse to the receiver period 511 shift register is produced. Thus the counter measures the time interval between the occurrence of a shift pulse in the transmitter coder and the very next shift pulse to occur in the receiver coder, which is to say, the displacement between the two codes modulo a full digit period, or $(M - m_1 \cdot t_d)$ μsec.

If the counter is programmed to count at the outputs of the two 125-μsec word detectors, then a *count* signal occurs every time the 125-μsec word detector in the transmitter coder pays off, and a *stop count* signal occurs each time that the 125-μsec word detector in the receiver coder pays off. Thus the counter measures the time interval between the occurrence of a 125-μsec word detector pulse in the transmitter coder and the next 125-μsec word detector pulse to occur in the receiver coder, which is the displacement m_3.

There are three flip-flop signals provided from the coder subsystem to facilitate use of the counter in coder checkout: *counting*, *shifting in progress*, and *in sync*. The *counting* signal, when true, indicates that the counter is presently in the process of completing a count. The *shifting in progress* signal, when true, indicates that shifting in some unit is presently in progress. If the coders have been programmed to complete a total number M of shifts, the *shifting in progress* signal will remain true until shifting in all three units is completed. This signal does not, however, indicate the occurrence of range rate shifts. Finally, the *in sync* signal, if true, indicates that the *count* and *stop count* signals to the counter are exactly in phase, or in sync. Since the in sync condition would yield a zero count in the counter, the *in sync* signal provides additional information when this situation occurs.

f. Control of coder subsystem by Mod III. A brief summary of application rules for using the coder subsystem is given in Table 2. Restrictions on the permissible magnitudes of certain of the words arise strictly from equipment limitations and do not represent theoretical limits of performance.

The coder subsystem is reset and started by separate commands from the Mod III. A *reset* signal, which must be "true" for no less than 100 μsec, resets the transmitter and receiver coders and zeroes the range rate register, the 1-μsec shift word (m_3) register, and the digit shift word (m_1) register. (When a coder is reset, the period 125 and period 511 shift registers are placed in the all 0's state, and the 125-μsec word detector accumulator is zeroed.) The clock number register, the S/T number register, and the counter are not affected by a *reset* signal. A *start* signal starts the transmitter and receiver coders running in phase. A *reset* signal must be given after a clock number and an S/T number have initially been loaded into the subsystem from the Mod III, and thereafter, following each change of either of these two numbers.

A summary of the various word input–outputs and flip-flop input–outputs between the coder subsystem and the Mod III is given in Table 3 which also shows the Mod III address assignment for each input–output.

Table 2. Application rules for planetary coders

1. $0 <$ clock number $\leq (2^{21} - 1)$
2. $0 <$ S/T number $\leq (2^{22} - 1)$
3. $-(2^{21} - 1) \leq$ Range rate $\leq (2^{21} - 1)$
4. 1-μsec shift number = any integer representable in the Mod III.
5. 125-μsec shift number = any nonnegative integer representable in the Mod III.
6. Digit period shift number = any integer representable in the Mod III.
7. Digit period = clock number • 125 μsec.
8. S/T number = the period of time between two successive range rate inputs to the NCO, expressed in units of 25 μsec.
9. Range rate = number of shifts desired per unit period of time. The shifts will be spaced approximately uniformly over that period. Positive rates correspond to *right* shifts.
10. Positive numbers as 1-μsec shift numbers will produce *right* shifts.
11. Positive numbers as 125-μsec shift numbers will produce *left* shifts.
12. Positive numbers as Dp shift numbers will produce *right* shifts.
13. The *reset* flip-flop must be set, then reset, to ensure that the reset condition lasts for at least 100 μsec.
14. The *start* flip-flop must be pulsed to get only one start signal inside the coders.
15. The flip-flops to designate which function the counter is to count may be either set and reset, or pulsed. The counter will not start counting until all flip-flops are false, and it will count the function designated by the last flip-flop to be true.
16. The *in-sync* signal tests the same function that the counter counts.

Table 3. Subsystem input–output

Inputs to coders (numbers)	Outputs from coders (numbers)
22230—1-μsec shift word (m_3)	20230—1-μsec shift word register
22231—125-μsec shift word (m_2)	20231—125-μsec shift word register
22232—1-Dp shift word (m_1)	20232—1-Dp shift word register
22233—	20233—Low-order counter
22234—Clock number	20234—Clock number
22235—S/T number	20235—S/T number
22236—Range rate	20236—Range rate
22237—	20237—High-order counter
Inputs (flip-flops)	**Outputs (flip-flops)**
23033—Count 125	21033—Counting
23034—Count digit	21034—
23035—Count 511	21035—
23036—Start	21036—Shifting in progress
23037—Reset	21037—In sync

g. Equipment. The planetary ranging coder subsystem consists of five blocks which contain digital logic modules. The logic modules used are Computer Control Co. Series-T digital modules. All logical operations are clocked by an internal 1-Mc clock which is derived from a 1-Mc station reference signal.

D. Lunar Radar Project

1. X-Band Lunar/Planetary Radar System

a. Introduction. The Goldstone Communications Supporting Research and Advanced Development effort has been expanded greatly by the inclusion of a 30-ft Az-El antenna at the Venus site. Work on this antenna (Fig. 23) is nearing completion and much of its progress has been reported in previous issues of *SPS* (Refs. 23 and 24).

With the increasing reliability and capability of the 85-ft Venus site radar, a greater number of missions has been required of the 85-ft antenna. Recent planetary and lunar radar experiments almost saturated the time available, and spacecraft commitments will impose similar traffic for operations in the near future. Planning for these programs indicated a need for capabilities of a different sort, and the 30-ft antenna was built, in part, to fulfill this need.

At present, a new X-band (8448 Mc) radar system (Fig. 24) is being designed for the 30-ft antenna. The over-all system is similar to the present lunar radar except for the antenna system, which is more like the planetary

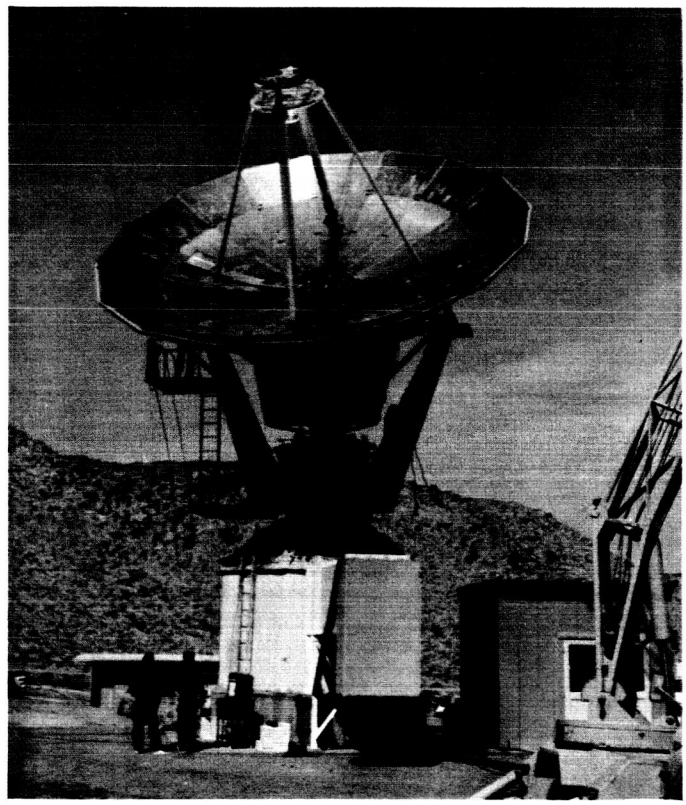


Fig. 23. 30-ft Az-El antenna

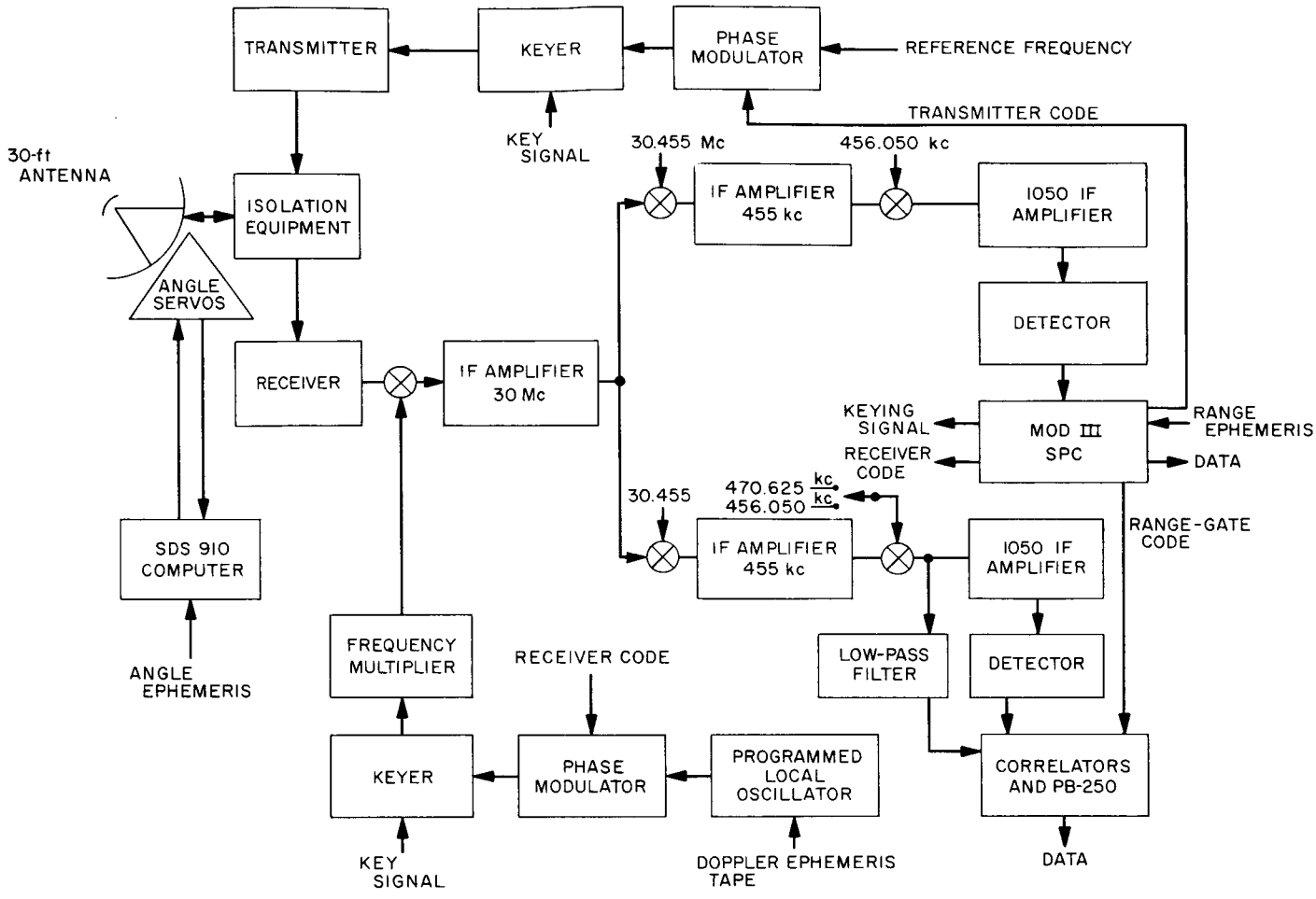


Fig. 24. X-band lunar/planetary radar functional diagram

radar. It will be capable of performing precision lunar range-gate radar experiments in a way almost identical to those now performed by the 85-ft antenna with several refinements, and it will be capable of providing coarse-tracking of the lunar surface to further reduce uncertainty in present lunar ephemerides. This tracking mode will be accomplished by biphase modulation of the transmitter and receiver local oscillators, just as the precision lunar mode, but differs in that tracking probably will be accomplished at lower digit rates, the return being correlated against two adjacent code phases. The difference between these two correlations provides the error-tracking curve. This differs from previous planetary tracking radars, wherein amplitude modulation was used, a clock-component in the code provided the S-curve, and in which much calibration difficulty was encountered.

Also, the 30-ft system will give the DSN extended capability for research and advanced development. The X-band radar will extend the frequency range of experimental and theoretical space communication studies so that together with the continuing 2.388-Gc work, we will essentially encompass the range of radio frequencies of probable future interest in Earth-space-Earth communications.

This new radar initially will have a sound capability on the Moon with considerable (8–15 db) future growth capability; also this initial capability predicts a satisfactory contact with Venus early in 1966.

b. Capability. The capability of the system is quite high. With a reasonable set of assumptions (Table 4), the basic capability may be normalized to 0 db. In these units the present lunar radar is −11.2 db. During the 1961 Venus conjunction, Jodrell Bank had +0.4 db, the MIT system had +1.7 db and the JPL radar was +11.2 db. The JPL radar moved, however to +14.2 db in the 1962 Venus experiment, and is now +26.0 db.

Table 4. Parameters of X-band radar

Item	Value
Frequency	8448 Mc
Gain	+56.2 db ($\eta = -2$ db, 63%)
Transmit loss	− 0.6 db
Net transmit gain	+55.6 db
Power transmitter	+69.0 dbm (8 kw)
Power density	+23.6 dbm/sterad
Effective receiver area	+16.2 db m^2 ($\eta = -2$ db, 63%)
Receive loss	− 0.3 db
Net effective area	+15.9 db m^2
Receiver system temperature	
T_{ant}	18°K
T_{feed}	20°K
T_{maser}	18°K
$T_{limiter}$	10°K
Total system temperature	66°K (18.2 db °K)
Frequency ratio $= f_s/f_e$	5.50 db
$[(f_s)/(f_s)]^{1/2}$	2.8 db

As mentioned previously, 8–15 db future growth capability is indicated.

c. System description. The X-band lunar/planetary radar is a flexible system which will enable experimentation for the purpose of advancing the art and techniques of radar communications, particularly as related to DSN programs, as well as gathering useful scientific information. Implemented as a separate and independent operating system, it will permit such experimental operations without disturbing the status of the DSN operational complex.

Radar on the 30-ft antenna at the Venus site will be a monostatic CW X-band radar capable of operation at lunar (and planetary) ranges. Initially, the Venus site will attempt to have a radar operating almost all of the time—either at S-band on the 85-ft antenna, or at X-band on the 30-ft antenna. No attempt will be made to have both operating simultaneously. There will be maximum sharing of equipment between the two radars. However, if tests show that simultaneous operation is feasible, equipment for simultaneous operation will be considered.

A digital complex serves in control, ranging-signal generation, computation, data recording and data processing functions.

Angle-pointing subsystem. An SPS 910 general-purpose computer will provide angle-pointing for the 30-ft antenna. This is a conceptual prototype for the DSN.

Transmitter subsystem. The transmitter itself will be capable of transmitting 25 kw. The power supply, however, will be one used for the S-band 10-kw transmitter. This combination will only supply about 8 kw of RF power. The power supply is the present limitation, as the tube is designed for 25 kw.

Receiver subsystem. Ranging will be accomplished by use of the pseudorandom code techniques previously developed at JPL and employed in planetary and lunar experiments. Phase modulation of the RF carrier will be used in tracking, rather than AM as used in previous planetary ranging. Range coding and signal processing will be carried out by the Mod III SPC with minor modification.

Signal processing subsystem. The present signal processing equipment (correlators and PB-250) will be used with only minor changes.

Additional description in greater depth will be given in subsequent reports.

2. X-Band Lunar Radar Transmitter

a. Introduction. An X-band transmitter operating at 8.448 Gc will be used for lunar studies in the initial installation in the 30-ft antenna at the Venus site. The transmitter will use the power supply and control circuitry formerly used on the Echo and planetary radar 10-kw S-band transmitter. The klystron, magnet, cabinet, exciter traveling wave tube amplifier and transmitter control components to be mounted in the antenna were supplied to JPL in a partially assembled state, following a contract cancellation. The wiring assembly and documentation of this equipment is presently being carried out at JPL.

A block diagram of the X-band transmitter showing equipment location (water system not shown) and function is shown in Fig. 25. A description of some of this equipment and intended modifications follows.

b. Klystron. A VA 849 klystron operating at 8.448 Gc will be used in the initial installation. The klystron is capable of delivering an RF power output of 25 kw with a beam power supply of 26 kv and 3 amp. The power supply to be used in this installation develops 17.5 kv at 2 amp providing a klystron power output of approximately 8 kw.

c. Traveling wave tube amplifier. A traveling wave tube (TWT) amplifier rated at 10-w output with minimum gain of 36 db will be used as the final amplifier in

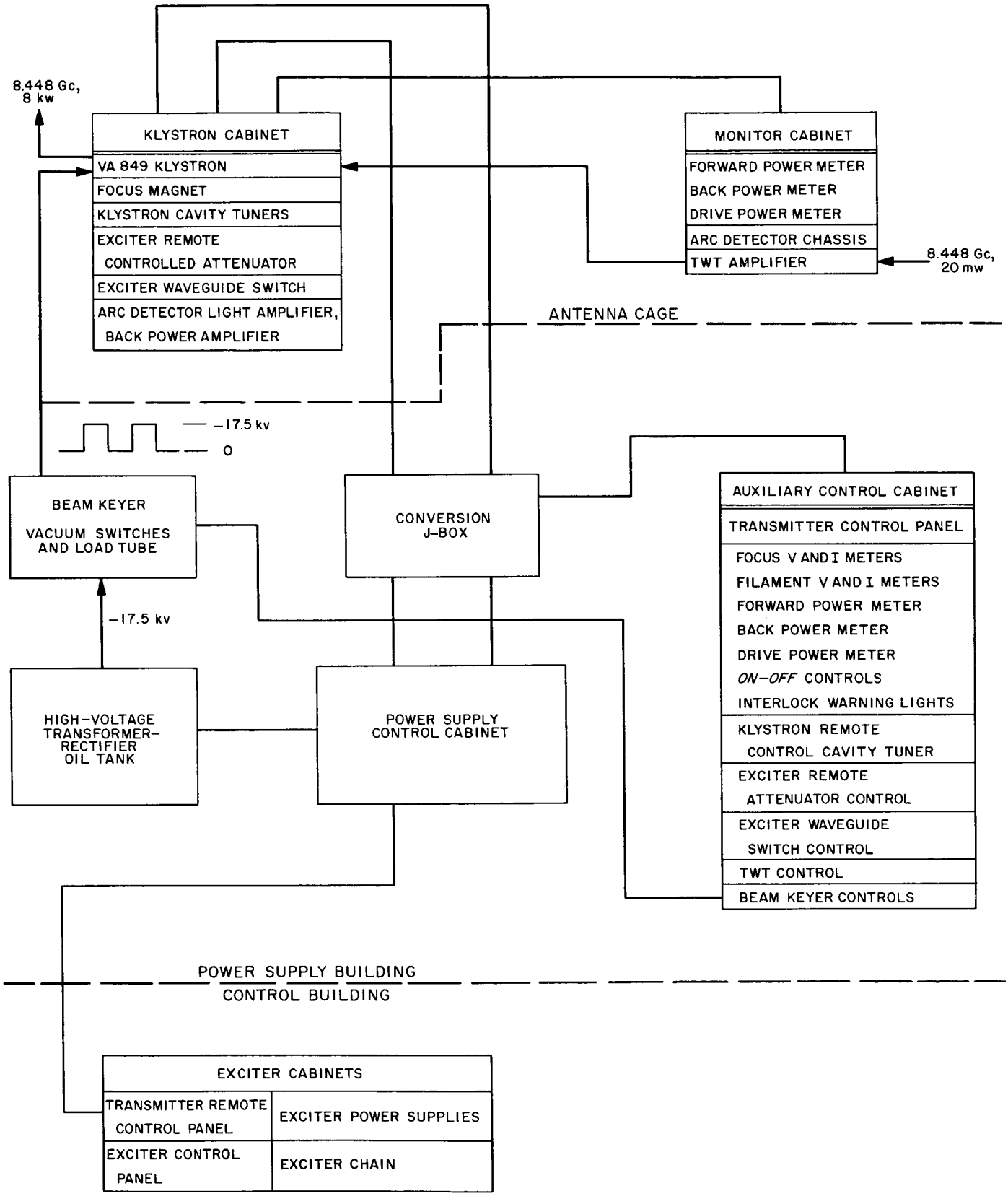


Fig. 25. X-band transmitter equipment location

the exciter chain. The water-cooled TWT, power supplies, meters and associated control circuitry are housed in a single water-tight box suitable for mounting in the antenna cage. This assembly will be mounted inside the antenna monitor cabinet for additional protection from the elements. Since the interconnecting line between the TWT amplifier and the klystron cabinet is only 5 ft, a semirigid coaxial cable having 0.12 db loss per foot will be used for the connection instead of lower loss rigid waveguide; only 4 w of power are needed at the input to the klystron cabinet. The front control panel of the TWT amplifier is shown in Fig. 26 and the partially assembled power supply subchassis is shown in Fig. 27.

d. Power supply. The principal modification to the existing beam power supply will be the addition and relocation of control circuitry. The old 10-kw S-band system had the klystron focus voltage and current meters, filament voltage and current meters, associated controls and interlock circuitry located in the antenna monitor cabinet. This added complexity and inherent unreliability to the system because of antenna vibration, various orientations and exposure to the elements. The new X-band system will have this equipment located in an auxiliary control cabinet in the power supply building.

e. Conversion J-box. The X-band klystron cabinet and monitor cabinet will be wired essentially the same as the present 100-kw S-band transmitter installed in the 85-ft antenna at the Venus site. This will permit the X-band transmitter to be used in either the 30-ft or 85-ft antenna with minimum modifications. For operation in the 30-ft antenna it will be necessary to have a conversion J-box located in the power supply building to make the antenna X-band transmitter equipment compatible in operation with the 10-kw S-band power supply.

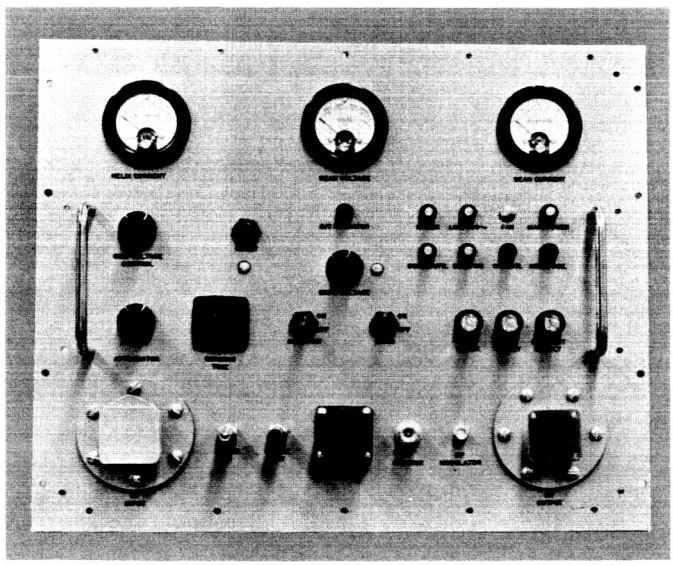


Fig. 26. Front control panel of TWT amplifier

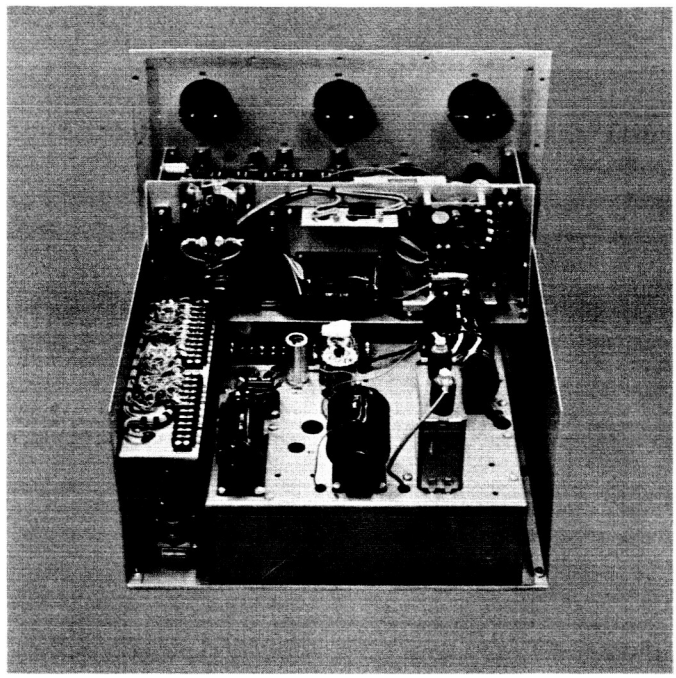


Fig. 27. Partially assembled power supply subchassis

3. Beam Voltage Keyer, 8.448-Gc Lunar Radar

a. Introduction. The beam voltage keyer will remove the high voltage from the klystron power amplifier in the 8.448-Gc radar transmitter during receiving periods. This will greatly reduce the noise generated in the klystron which would otherwise degrade the receiving system noise temperature. A klystron amplifier is a strong source of noise when operated with beam voltage but no signal excitation. Fluctuations in the number of electrons emitted by the cathode (shot effect) are amplified 40–50 db by the tube and the resultant noise output will saturate a receiver operating within the klystron bandwidth (Refs. 25–27) for similar measurements on S-band klystrons.

Stability of the high-voltage power supply will be improved by switching to a static load simultaneously with the removal of the voltage from the klystron. A hydrogen thyratron will discharge the energy stored in the 200-ft cable connecting the power supply and klystron in order to reduce the "fall" time of the beam voltage pulse. High-voltage vacuum relays will be used for beam switching.

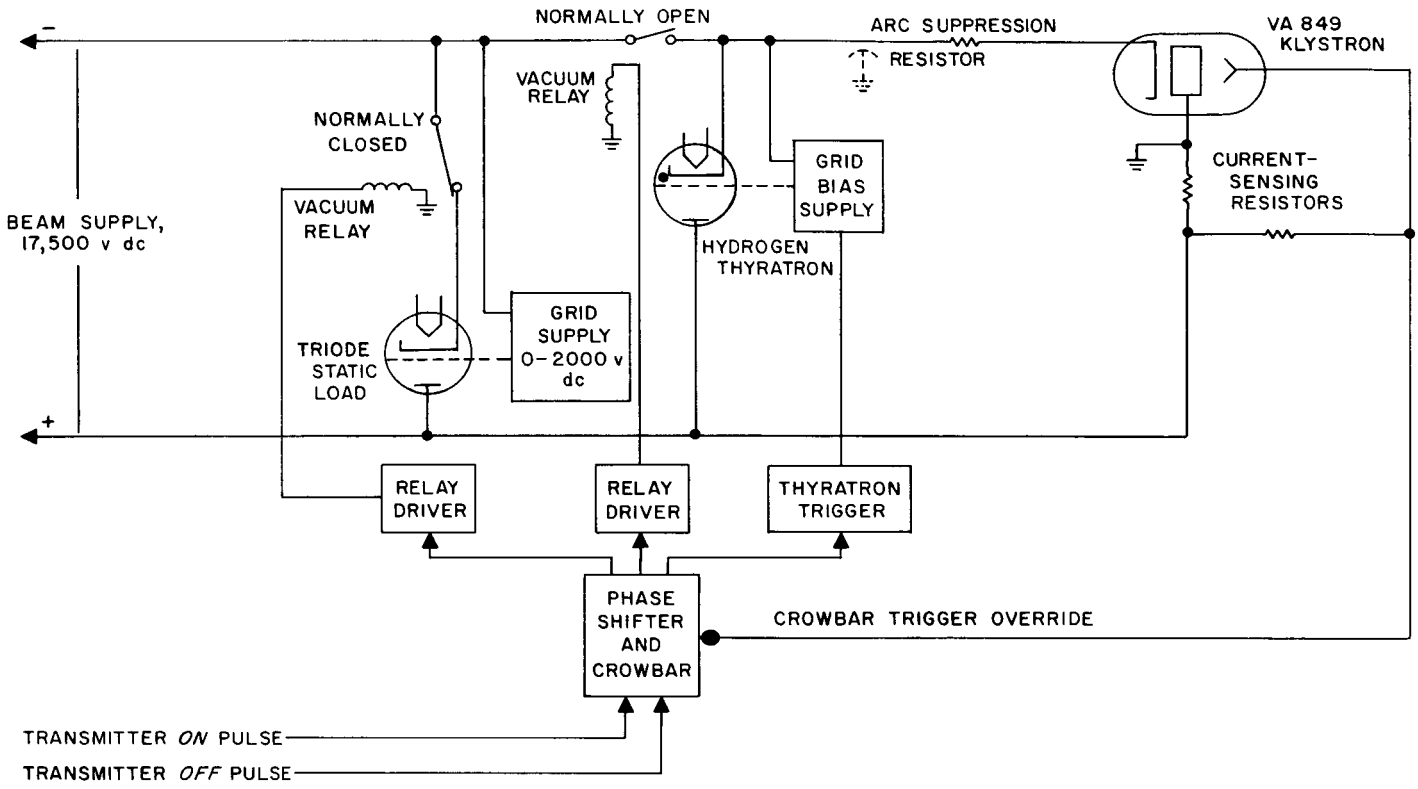


Fig. 28. Beam voltage keyer, X-band lunar radar

The keyer will also be connected as a crowbar for klystron protection in the event of an internal arc.

A simplified schematic diagram of the beam keyer is shown in Fig. 28. With no keying signal, or during the receive mode, the beam supply is connected to a water-cooled, transmitting-type triode tube through the normally closed contacts of a high-voltage vacuum relay and the klystron is disconnected, providing "fail-safe" operation. The triode tube is used as a static load on the power supply. By adjusting the grid voltage, the plate current may be set so as to maintain the same load on the power supply during transmitting and receiving cycles. Beam voltage "droop" or rise during the transmitting period will result in RF signal phase shift due to the 1 rad/kv pushing factor of the VA 849 klystron. To transmit, the normally open vacuum relay is closed, applying voltage to the klystron and the load triode is simultaneously disconnected. At the end of the transmitting cycle, the relays are deenergized and the thyratron is fired, discharging the high-voltage line. To compensate for variations in relay operate times, four separate, adjustable time-delay controls are provided, one each for the leading and trailing edges of both the transmitter *on* and transmitter *off* pulses. Crowbar operation will be provided by an "override" on the relay and thyratron controls to remove the beam voltage from the klystron when an internal arc occurs.

4. X-Band Receiver

a. Introduction. Modifications and additions to the present S-band Mod IV receiver required for X-band operation in conjunction with the 30-ft antenna consist essentially of adding an X-band local oscillator multiplier chain and a receiver antenna box containing the X-band to 30-Mc conversion equipment. Loop bandwidth considerations and input switching will require minimal modification. Fig. 29 shows the relationship of the planned revised receiver to the existing installation. Principal areas of interest are discussed here.

b. S-, X-band switching and frequency control. In the interest of minimum additional hardware requirements, including the use of the present basic programmed local oscillator, it is planned to utilize the existing 31.44-Mc receiver VCO and programming by providing a frequency offset of 3.635 Mc at the output of the programmed local oscillator. This will provide the required 35.075-Mc nominal input to the X-band multiplier chain. The selection

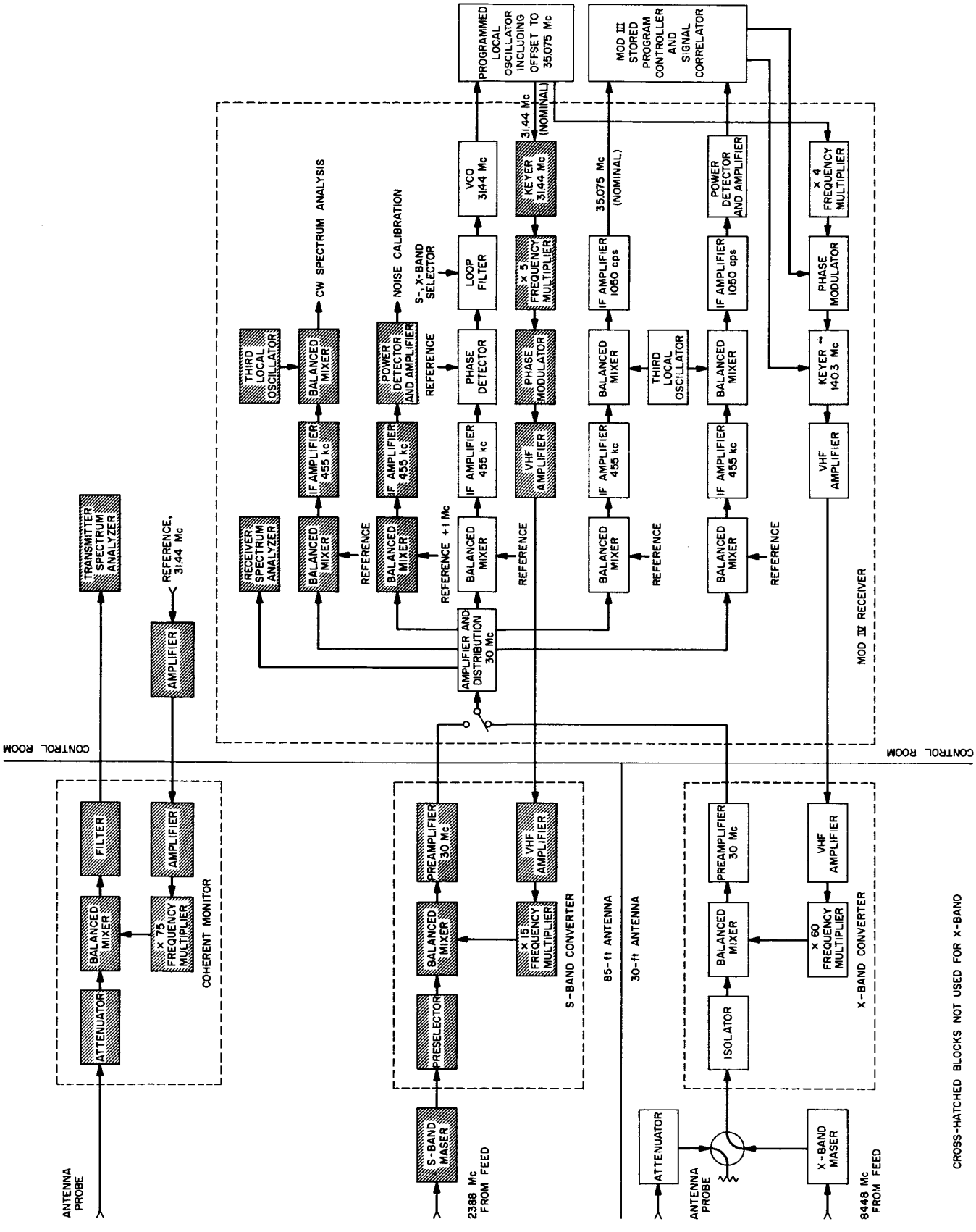


Fig. 29. X-band receiver, simplified block diagram, overlaid on existing S-band

of tracking, programmed or fixed (reference) drive to the S- or X-band multipliers is expected to be accomplished at the programmed local oscillator. Further detail on the latter device is separately reported.

The receiver closed-loop phase gain will then be altered only by the new local oscillator multiplication factor of 240. This represents an increase in gain of 240/75 as compared to the S-band system. In order to maintain the same nominal loop bandwidth ($2\beta_{L_O}$) selection of 5, 10, and 20 cps, corresponding alteration of the time constants of the loop filter is required.

Utilizing present techniques and hardware, it is doubtful that a maximum over-all system phase error (due to oscillator and multiplier phase instabilities) of 3 deg rms can be met at bandwidths much narrower than 10 cps. Extrapolating the Mod IV S-band system jitter of 2.7 deg at $2\beta_L = 5$ cps by the square root of the frequency ratio of 8448/2388, approximately 5 deg rms would be expected for this bandwidth. Similarly, measured S-band jitter of 1.4 deg at $2\beta_L = 10$ cps would predict 2.7 deg rms at X-band.

c. New hardware. New solid-state multiplier chains are being designed and procured for both the receiver and transmitter exciter. Referring to Fig. 29, this includes frequency multiplication of $\times 4$, phase and keying modulation at VHF, amplifiers and $\times 60$ to X-band. These components are reported separately.

Waveguide switching is planned for injection, after the maser, of a sample of transmitter power for spectrum analysis. Thus, in the test mode the transmitter spectrum will be detected by the complete receiver, rather than by means of a "coherent monitor" as used at S-band.

The X-band converter or receiver front end will be conventional in configuration. The inherent selectivity of the maser precludes the requirement of a band-pass preselector preceding the X-band mixer. An isolator at this point in the system is planned to optimize impedances as "seen" by the maser and the mixer input. The balance of mixer diode currents has in the past been strongly dependent upon proper impedance presented to the mixer signal input port, particularly when preceded by a preselector tuned to the signal frequency (thus presenting a reactive impedance at the local oscillator injection frequency). The use of the isolator is intended to solve this problem, as well as stabilize maser performance.

An X-band integrated mixer/preamplifier of the same type as was planned for the S-band monostatic satellite and lunar radar (MSSLR) system is on order. Availability and physical size are attractive. Noise figure, power gain and bandwidth are rated almost identically with the S-band unit reported in Ref. 28.

5. Multiplier Chains

a. Introduction. Three complete multiplier chains, one each for transmitter exciter, signal generator, and receiver local oscillator (LO) have been designed and are in procurement for use on the X-band lunar radar. A basic multiplier chain has been developed. It will cover the design requirements of all these chains and also will be suitable for the generation of S-band signals should conversion to all solid-state be required on that system in the future. Each chain is capable of digital phase modulation and keying.

b. Basic multiplier chain. A total of four frequency multiplier chains is required for the generation of X-band signals for:

(1) The transmitter exciter.

(2) Standard signal generator.

(3) Receiver LO injection.

(4) Transmitter monitor LO injection. For the present, it is contemplated to switch the main receiver components to provide this facility and to add a separate monitor at a later date.

A block diagram of the basic frequency multiplier chain developed for use in all cases is shown in Fig. 30. In order to reduce the total number of module types, functionally similar subunits have been standardized so that their range of adjustment is adequate to cover the design requirements of all chains. Moreover, in the event that conversion to all solid-state will be required at some future date, these modules also can be used on the S-band system.

Each chain has provision for phase modulation and keying of the output frequency. These functions are performed immediately after initial frequency multiplication, the remainder of the multiplication being located at the antenna. VHF amplifiers, of the amplitude limiting type, are included at each end of the connecting cable run to make up for losses. All antenna-mounted equipment is housed in JPL standard RF and weather-tight boxes.

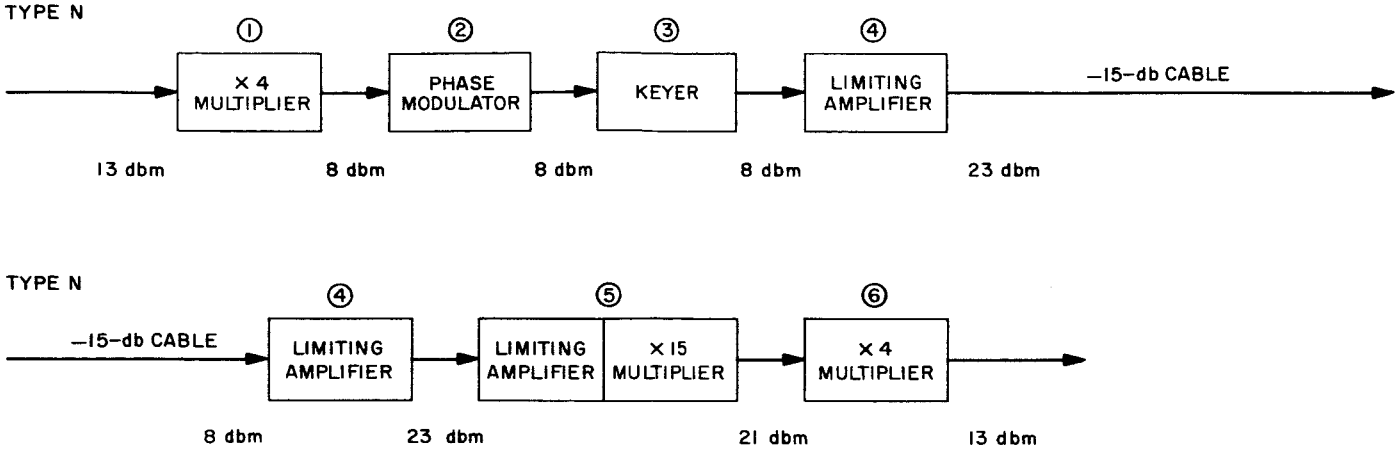


Fig. 30. Basic X-band multiplier chain

Table 5 lists the frequencies to which each of the module types have to be tuned for X-band (and also for S-band) operation. Module type No. 1 operates at a nominal input level of 13 dbm and provides initial ×4 multiplication on X-band (or ×5 on S-band) at an output level of 8 dbm. Phase modulation and keying provided by module types No. 2 and No. 3, respectively, operate at unity gain so that either of these functions may be duplicated or deleted without changing the operating power level of the remainder of the chain. Amplitude limiting amplifiers type No. 4 provide a gain of 15 db at nominal input. The first amplifier is included to make up for the 15-db cable loss between control room and antenna, the second to make up part of the total insertion loss associated with the over-all frequency multiplication. The remainder of the power gain required to obtain an X-band output of 13 dbm is provided by an amplitude limiting amplifier in the ×15 frequency multiplier, type No. 5. Final ×4 frequency multiplication to X-band is provided by module type No. 6, or S-band output frequencies may be obtained at the output of the ×15 multiplier by appropriate tuning.

Table 5. Module operating frequencies

Type No.	X-band frequency, Mc		S-band frequency, Mc	
	Transmitter	Receiver	Transmitter	Receiver
1. Frequency multiplier	35.2	35.075	31.84	31.44
	140.8	140.3	159.2	157.2
2. Phase modulator	140.8	140.3	159.2	157.2
3. Keyer	140.8	140.3	159.2	157.2
4. VHF amplifier	140.8	140.3	159.2	157.2
5. Frequency multiplier	140.8	140.3	159.2	157.2
	2112.0	2104.5	2388	2358
6. Frequency multiplier	2112.0	2104.5	Not used	Not used
	8448.0	8418.0	Not used	Not used

c. Amplitude stability. For an input power variation of ±1 db the electrical design requirements of individual modules have been specified so as to meet a target stability of ±2 db at the output frequency. However, the degree of amplitude limiting called for has been kept to the minimum required to avoid deterioration of *on–off* ratios of the keying function.

d. Phase stability. Since these chains are used to generate signals which are required to be phase coherent with extremely phase-stable inputs, the electrical design has been directed toward minimizing the phase-shift contributions of the various modules.

Variations in ambient temperature conditions constitute the major cause of phase shift. Contributing factors include variations in RF drive changing load conditions, and imperfections of terminal match conditions. These effects have been minimized by the use of transitionally coupled band-pass filters as coupling elements. Changes in load conditions are swamped by means of resistive loading, and a bandwidth sufficient to accommodate the drift in center frequency has been specified so that a target over-all phase stability of 15 deg/°F may be obtained.

e. Phase modulation. The modulation process used in these chains is essentially binary in character. This calls for a digital-type phase modulator capable of being preset to a desired value of modulation index. This latter should be, ideally, independent of the modulating signal amplitude and the transition between the two peak modulation depths should be as abrupt as possible.

The modulator is required to operate from a square-wave modulating signal having peak voltage amplitudes

of -0.5 ± 0.2 v and -1.5 ± 0.2 v, rise and fall times of 50 nsec and a mark-space ratio of unity. Phase modulation is performed at one-sixtieth of the output frequency and may be preset to any depth between 20 and 180 deg peak-to-peak at the output frequency by means of two adjustment controls, a coarse step control and a continuously variable fine control.

The lighter modulation depths are used to apportion the main carrier and sideband energies so that the main carrier and code clock loops may operate at similar receiver thresholds. The maximum phase modulation of ± 90 deg is used when the sideband energy is required to be a maximum. In this application the carrier is subsequently reconstructed by beating the received signal with a replica of the transmitted signal, the phase of which has been suitably delayed for the purpose of assessing signal plus noise and also range. Since any residual carrier will contribute toward the noise output, a high degree of carrier suppression is desirable. In this respect a target carrier suppression of 50 db has been established. This calls for a deviation stability of 0.12 deg in 90 deg; that is 0.13%. Asymmetry of the square-wave modulation will also increase the residual carrier so that a tolerance of $\pm 0.1\%$ has been specified for the unity mark-space ratio.

Fundamentally, bistate modulation may be achieved by either of two methods: (1) digitizing a standard linear phase modulator by amplitude limiting the input modulation, or (2) selecting either of two modulation states by means of a switch. While the first method could utilize existing equipment, investigations along the lines of the second method were considered more profitable due to the inherently greater stability of a fixed as opposed to a variable phase-shift device.

Fig. 31 indicates various ways in which bistate modulation may be switched. Arrangements (a) and (b) meet the basic requirements. The phase stability associated with the individual elements consists of two components: (1) a purely random change in phase, and (2) a drift in phase that is some function of external influences such as temperature, operating conditions, etc.

In Fig. 31 (a) the instantaneous values of the first component add arithmetically in the two channels to give a peak-to-peak phase stability that will be inferior to that of Fig. 31 (b). On the other hand, arrangement (a) of the figure could be superior to arrangement (b) with respect to the effect of the second component, since tracking of elements $+\phi$ and $-\phi$ in (a) can be expected to materially reduce the over-all effect.

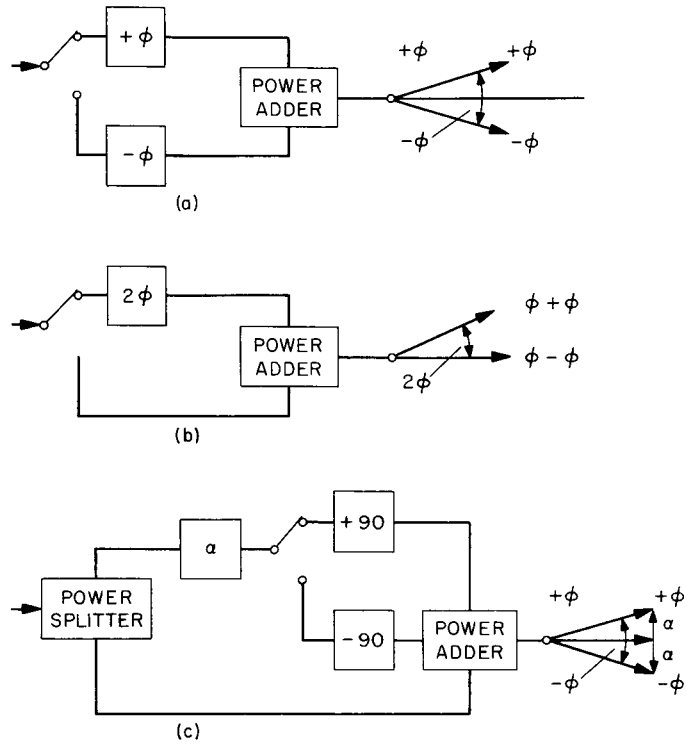


Fig. 31. Bistate phase modulators

This is of considerable importance. For ± 90-deg phase modulation of the output frequency, $\phi = 1.5$ deg and the over-all phase stability would have to be ± 0.002 deg over the full range of environmental conditions: a rather stiff requirement.

This situation may be relieved considerably by the arrangement of Fig. 31 (c). In this case the main carrier is deviated by the addition of a suitably attenuated quadrature component as shown in the vector diagrams, and the burden of achieving the desired phase-shift stability is now essentially transferred from the phase-shift elements to the attenuator element.

A schematic diagram of a practical application of this principle is shown in Fig. 32.

Transistors Q1–Q3 are identical unity gain linear amplifiers whose output collectors are connected in parallel to the output load via a band-pass filter, T2. Each amplifier is stabilized with respect to gain and input impedance by means of heavy emitter degeneration and resistive swamping of the relatively high input resistance, respectively.

Either Q1 or Q2 is rendered nonconductive, alternately, by the push–pull modulating signal via an isolating dc

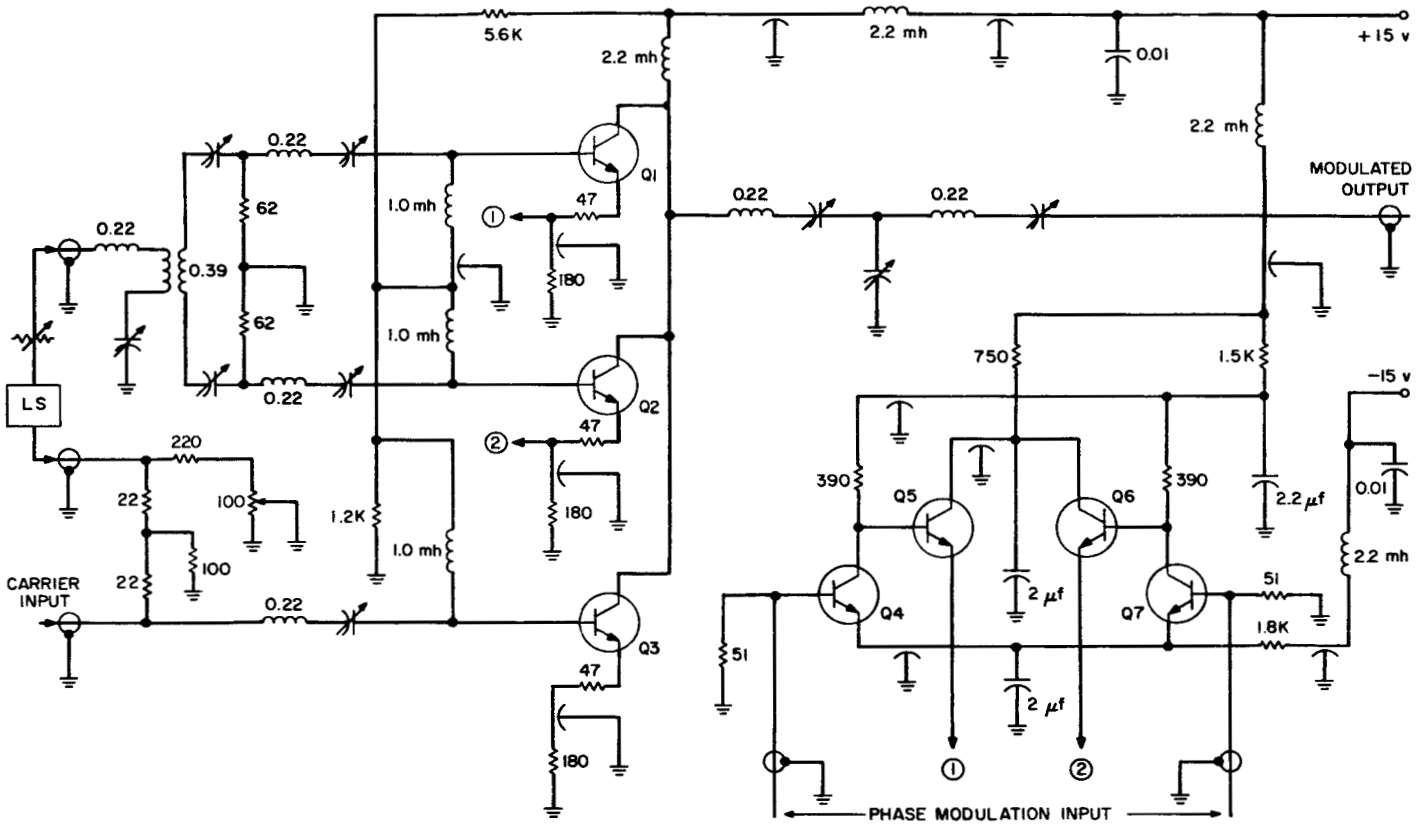


Fig. 32. Digital phase modulator

flip-flop driver formed by Q4–Q7. The input carrier is applied to the base of the main channel Q3 and a small portion is also fed to the double-tuned band-pass filter T1 via an external attenuator. The base inputs of the gain-controlled amplifier channels Q1 and Q2 are fed in push–pull from the secondary of T1 and hence at ±90 deg with respect to the primary of T1. In this setup, the inclusion of a line stretcher was found necessary to compensate for the delay in the external attenuator connections.

Electrical tests in the laboratory and at Goldstone have shown satisfactory operation. Carrier suppression has been maintained between 50 and 60 db and the major portion of this variation appears to originate in the external connections to the attenuator. A prototype is near completion for installation at Goldstone at which time a more protracted study will be made.

In the event that the differential gain variations among Q_1, Q_2, and Q_3 prove unacceptable, closed-loop operation may be considered. In this case the gain of Q_1 and Q_2 may be controlled by an error signal to maintain the correct modulation index.

6. Programmed Local Oscillator

a. Introduction. The S-band programmed local oscillator will be modified to furnish the requisite frequencies for either S- or X-band, selectable by means of a switch. This is to be accomplished by shifting the S-band frequency (31.44 Mc) to the X-band frequency (35.075 Mc) in a new type of balanced mixer (described in the following subsection 8 of this article).

b. Description. The output frequency of the S-band programmed local oscillator (PLO) will be shifted to the required frequency for X-band operation by adding 3.635 Mc output frequency to obtain 35.075 Mc (Fig. 33). This will be accomplished in the new model balanced mixer in order to eliminate the need for another frequency shifting phase-locked loop within the PLO.

Two additional frequency multipliers will be added to the PLO in order to obtain the programmed doppler for digital local oscillator control feedback. The frequency multiplication will be 240, the same as that in the PLO chain so as to produce the actual doppler at X-band for the digital control.

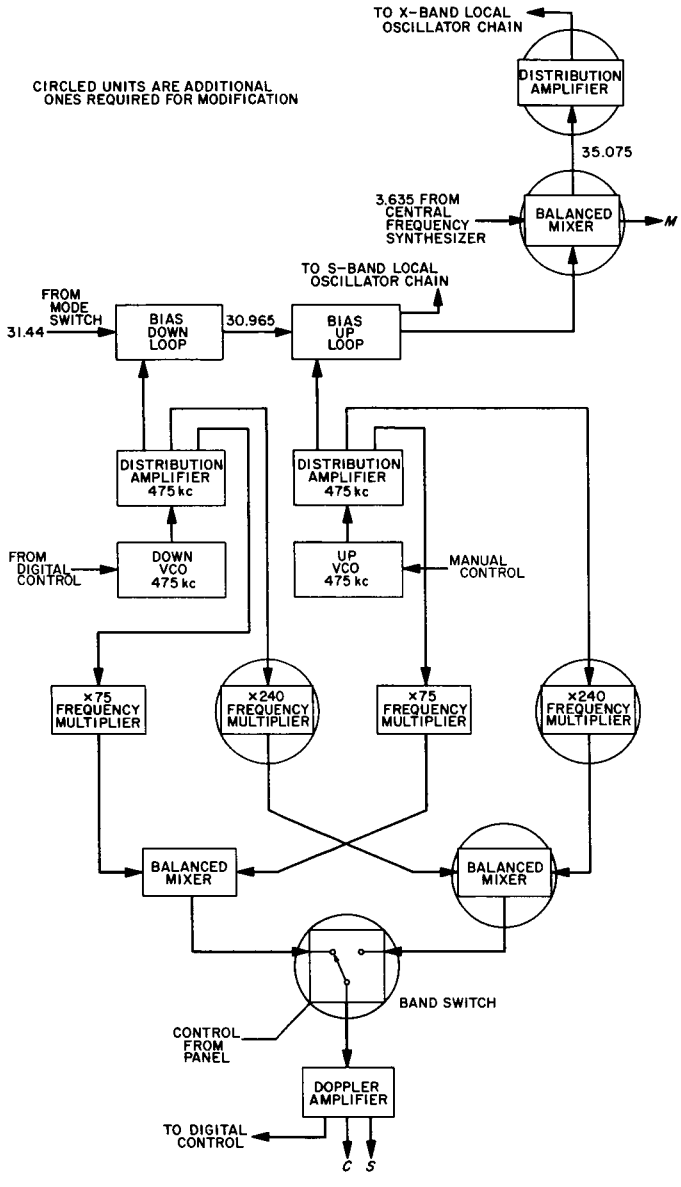


Fig. 33. Modification of programmed local oscillator for X-band lunar radar

Both the S- and X-band outputs will be available at all times, independent of the radar system operating mode. With this feature, tests of interaction of the S- and X-band transmitters and receivers may be made at any convenient time.

7. S- and X-Band Interim Frequency Synthesizer

a. Introduction. The X-band lunar radar will require frequency synthesizing equipment in addition to existing equipment. Plans for a permanent central frequency synthesizer have already been presented (Ref. 29). However, as a temporary expedient, an interim frequency synthesizer will be constructed. Using in part existing frequency synthesizing equipment now in the Mod IV receiver and exciter, the interim synthesizer will consolidate all frequency synthesizing equipment in one set of racks. After becoming operational on September 1, 1964, this system will function until the permanent central frequency synthesizer is constructed and becomes operational.

b. General description. Starting point for the system is a rubidium vapor frequency standard which provides a highly stable 1-Mc reference signal for all subsystems. The synthesizing equipment shown in Fig. 34 provides phase-coherent reference signals for both S- and X-band operation of the transmitter and receiver. Although only X-band operation is planned, the S-band capability is maintained at no additional cost since the modules already exist in the Mod IV exciter and receiver.

The synthesized frequencies divide into approximately three groups: S-band, X-band and IF. The S-band frequencies are 31.84 Mc for the exciter and 31.44 Mc for the receiver. The analogous X-band frequencies are 35.2 Mc for the exciter and 35.075 Mc for the receiver. The IF frequencies are utilized in the receiver channels (Ref. 30) and are 455 kc, 30.455 Mc, and 31.455 Mc. The output at 3.635 Mc is utilized by the programmed local oscillator (subsection 6 of this article).

Since the parts of this system were originally designed independently of one another, the method of synthesis is not optimum. The lack of phase coherency of the 455-kc reference signal is a disadvantage inherited from the Mod IV synthesizing equipment. A 30.455-Mc synthesizer has been purchased from Montronics, Inc. If it meets system specifications, it will replace the indicated modules in Fig. 34. Then a phase-coherent 455-kc signal can be obtained using a 30-Mc signal, the 30.455-Mc synthesizer, and a 455-kc balanced mixer.

c. Equipment. The rubidium standard to be used will be the standard now housed in the exciter racks at the Venus site. As shown in Fig. 34, the interim system makes use of 22 modules from the receiver and 18 modules from the exciter. The remaining 16 modules must be built or purchased. The majority of these new modules provide the X-band frequencies and will be used subsequently in the permanent central frequency synthesizer. The 3.635-Mc and 35.075-Mc balanced mixers are built from a new design which is discussed in subsection 8 of this article.

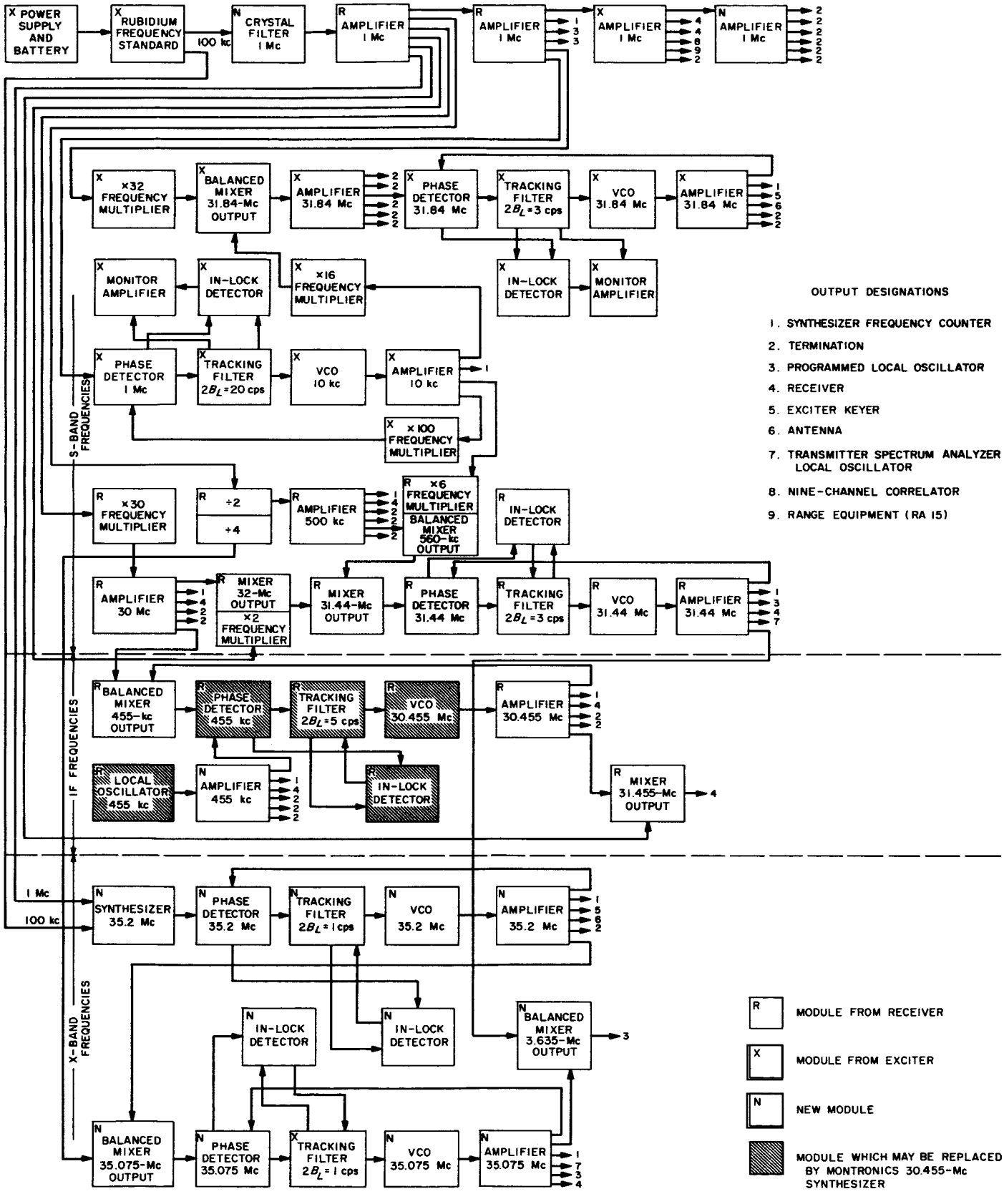


Fig. 34. S- and X-band interim frequency synthesizer

The interim synthesizer will occupy two adjacent racks. One will contain two vertical cold plates mounted on sliders for the modules. The other rack will contain the rubidium standard and its power supply, the module power supplies mounted on a water-cooled cold plate, a frequency counter, an oscilloscope, and switching and control panels.

8. 30.455-Mc Balanced Mixer

a. Introduction. The 30.455-Mc balanced mixer was developed to improve on the previous vacuum tube model which suffered from low-level outputs, insufficient gain, and high-level spurious sidebands.

This particular mixer will be used to implement the S- and X-band central frequency synthesizer.

Specifically, this mixer accepts 30.0 Mc and 455 kc, mixes the two signals in a balanced arrangement, and produces the desired 30.455 Mc.

The module is a gold-plated, cavity type of the mechanical configuration suited to the existing 2388-Mc planetary radar receiver located at the Goldstone Venus site.

b. Function. The balanced mixer (Fig. 35) consists of one 30.0-Mc amplifier-limiter input stage, one 455-kc amplifier-limiter input stage, a two-transistor balanced mixer section, one 30.455-Mc crystal band-pass filter, a two-stage output amplifier section and an RF diode detection circuit. The circuit diagram is shown in Fig. 36.

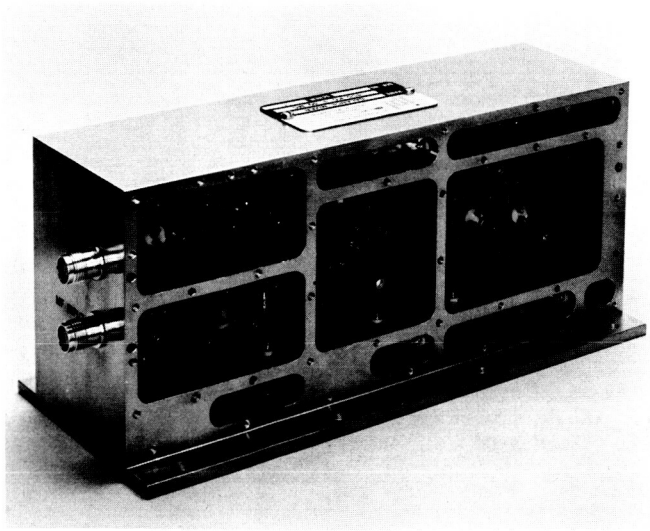


Fig. 35. 30.455-Mc balanced mixer

The VHF and MF input impedances were designed for a nominal 50 ohms, and this impedance was measured at three separate levels (Fig. 37). The input voltage has been nominally set at +13 dbm for both inputs. The output voltage is +13 dbm, −0, +4 dbm into a measured 51-ohm impedance.

Variation of the output voltage versus the power supply voltage is shown in Fig. 38. It is interesting to note that although the module may suffer a 29% loss of dc input voltage, the usable output is still above +13 dbm.

The limiting characteristics of this mixer are presented in Fig. 39 (a), (b), and (c). In Fig. 39 (a) constant 455-kc input level was maintained, while the 30.0-Mc input was varied in 3-db steps (solid curve). It can be seen that the output held at +16.5 dbm for an input decrease of 21 db. Furthermore, an input decrease of 35 db still produced a usable output of +13 dbm. Fig. 39 (a) shows a broken curve indicating that the 30.0-Mc input was held constant while the 455-kc input signal was varied in 3-db steps. A 455-kc input signal decrease of 40 db still produced a +13-dbm output. Fig. 39 (b) shows a simultaneous decrease of both input signals. With each input signal attenuated 27 db, the output signal was still usable at +13 dbm. Fig. 39 (c) shows the RF detection curve which demonstrates the conventional limiting characteristics of this mixer. This output is used as a VTVM test point to check both input drive signals during the system maintenance.

The bandwidth of the mixer, which is determined by the bandwidth of the crystal filter, is 40 kc at 30.455 Mc. The output spectrum contained no measurable 30.00 Mc or 455 kc. The only spurious signal observed was at 30.2 Mc at −117 dbm.

The RF leakage of 30.0 Mc, 455 kc and 30.455 Mc was checked at input and output terminals (TNC jack), B+, monitor connector and external plate-to-plate mechanical junctions. In all cases, the RF leakage was found to be $\leq$0.6 μv. The mechanical chassis cavity design is credited for the low leakage (Fig. 35).

The module was subjected to a temperature test from +5 to +45°C. No thermal runaway was observed. The curve of output volts versus temperature may be seen in Fig. 40.

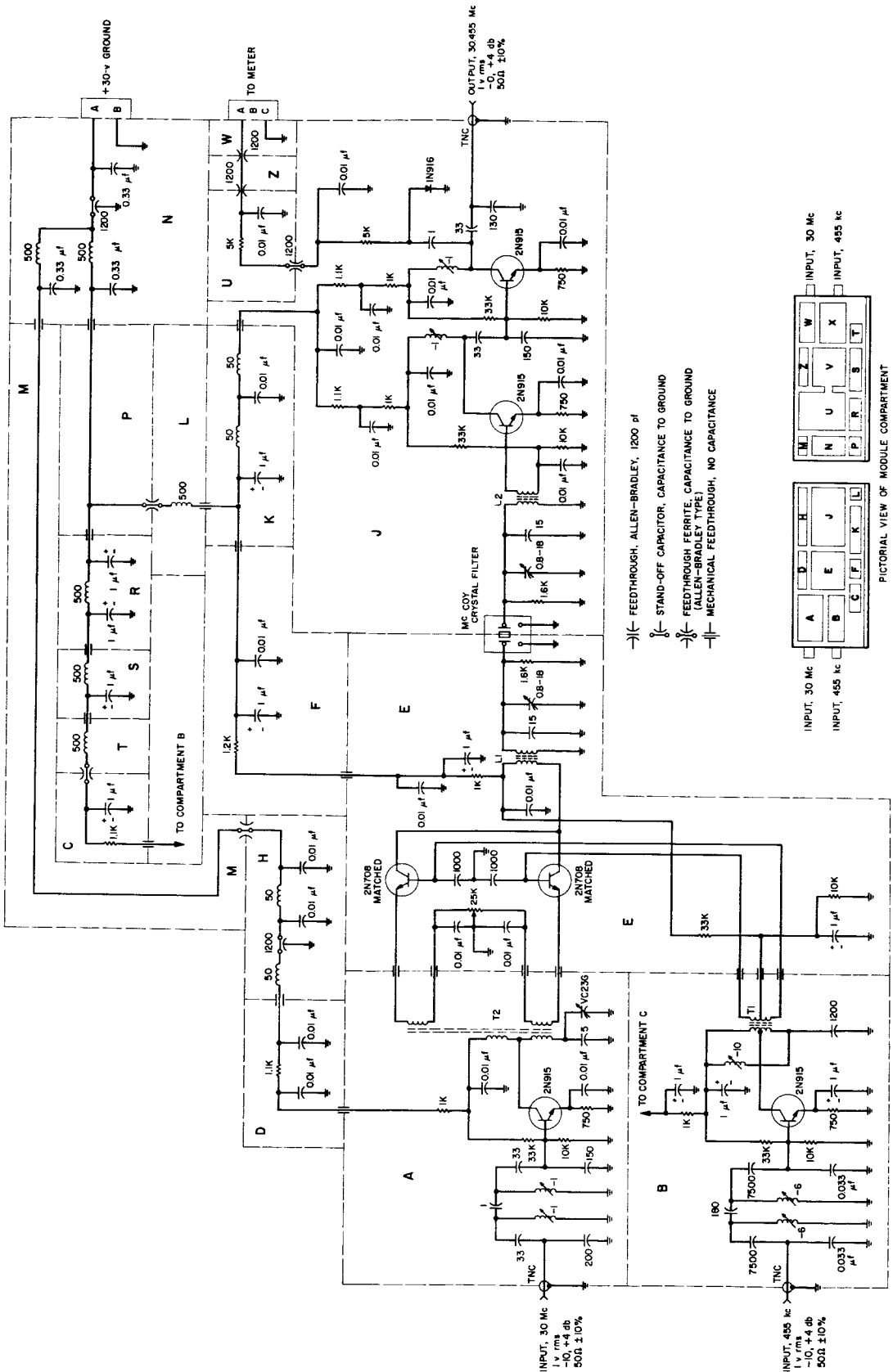


Fig. 36. Circuit diagram of balanced mixer

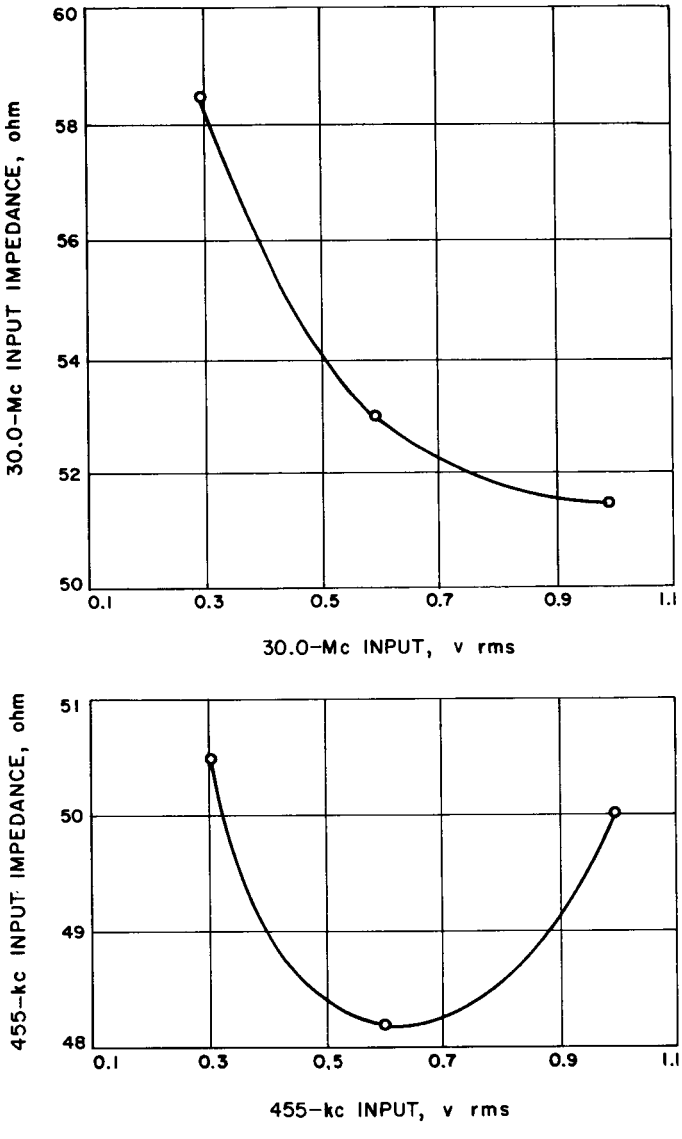


Fig. 37. Input signals versus input impedance

c. Conclusion. Future tests of this mixer include installation into the central frequency synthesizer at the Venus site. Two other balanced mixers of this configuration are presently being fabricated and should provide additional background data. The module is of all solid-state circuitry with emphasis on conservative design, simplicity, and ease of operation.

9. 8.448-Gc Standard Signal Generator

a. Purpose. A requirement exists for simulation of received transmitter signals for system test, calibration and checkout; and for measurement of receiver performance characteristics.

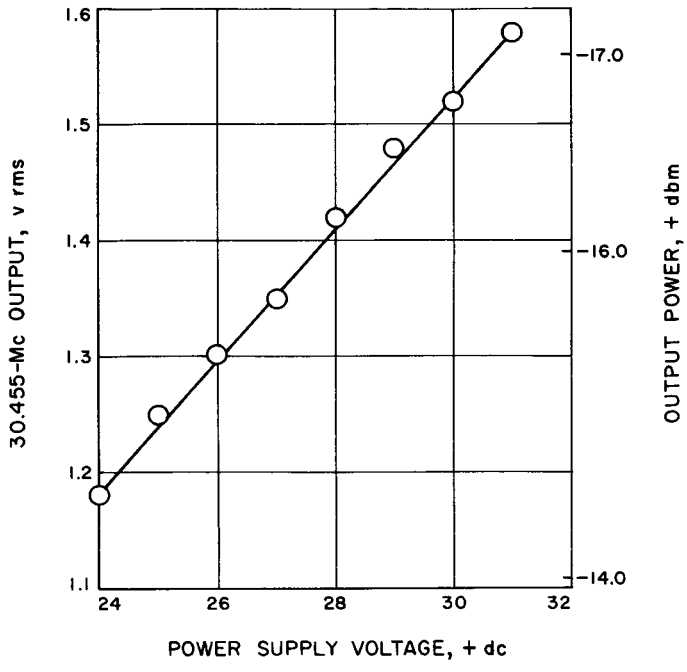


Fig. 38. Power supply variations versus 30.455-Mc output

b. General description. The 8.448-Gc (X-band) standard signal generator is an extremely stable, low phase-jitter, solid-state, signal source with *on–off* keying and pulse-code phase modulation capabilities thus having, essentially, all the characteristics of the X-band transmitter, except the high-power functions. In addition, the generator is capable of producing a range of precisely calibrated very low-level signals (down to approximately −180 dbm). Spurious radiation and leakage must be held to a level which cannot be detected in the receiver.

Since no commercial equipment is available to meet these requirements, the generator is being designed and built at JPL.

The principal characteristics of the X-band generator are:

c. Performance characteristics.

(1) [1]Output center frequency: 8.448 Gc/sec, controlled by a crystal-stabilized VCO.

(2) [1]Electronic tuning range: ±0.177 Mc/sec.

[1]Characteristics (1), (2), and (3) relate to operation with self-contained VCO. Optional selection of external system coherent doppler-error reference is provided.

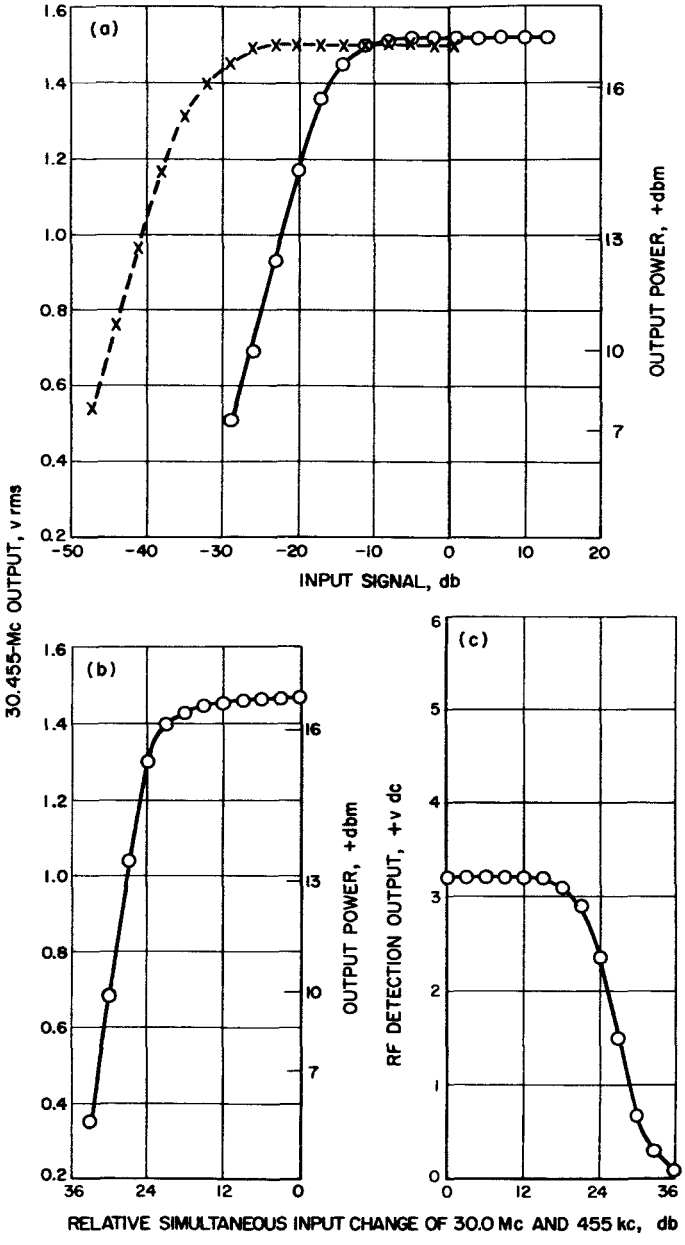


Fig. 39. Limiting characteristics

(3) [1]Frequency stability: 1 part in 10^9 for 1-min duration.
2 parts in 10^9 for 1-hr duration.

(4) Phase stability (unmodulated signal):
0.7 deg rms for $2B_{L_0} = 20$ cps (2 VCO's in measurement)

1.3 deg rms for $2B_{L_0} = 10$ cps

3.8 deg rms for $2B_{L_0} = 5$ cps

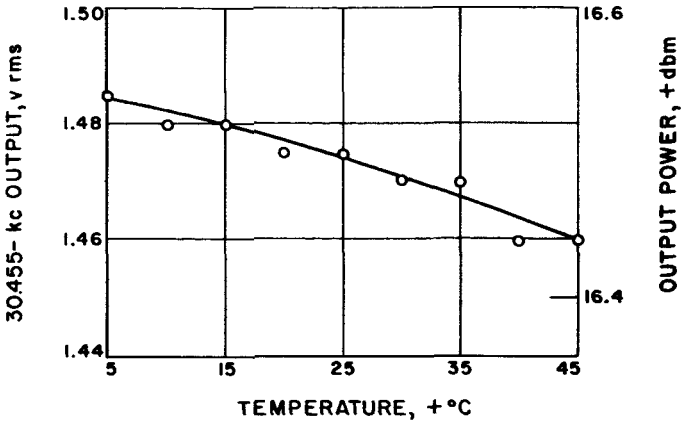


Fig. 40. Temperature versus output

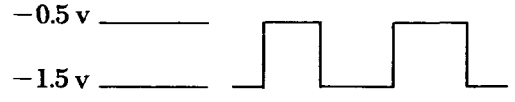
This data is based on phase error (jitter) characteristics of stable VCO's currently used at S-band. Phase error values are extrapolated proportionately to the square root of the frequency ratio for X-band.

(5) Power output: −80 to −180 dbm continuously variable, direct-reading. Accuracy: ±0.5 db throughout range.

(6) Phase modulation–pulsed:

Output: Phase shift adjustable between ±10 and ±90 deg, accomplished by use of a digital-type, bistate (nonlinear) device.

Input: Standard Range Code or Range Gate pulse train at levels shown below:



(7) Amplitude modulation–pulsed. Used for *on–off* keying at rates varying from 0 to 1000 cps. Duty cycle ratio of output signal and repetition rate determined by input control signal (levels same as for phase modulation input shown above).

d. Description of circuit. Fig. 41 is a functional block diagram of the 8.448-Gc standard signal generator.

A stable VCO (of the type described in Ref. 31) is incorporated as a self-contained stable signal source. Provision is also made for substituting an input from the system coherent reference at 35.2 Mc. This latter is an external VCO signal, phase-locked to the rubidium vapor maser frequency standard. The VCO generates nominally

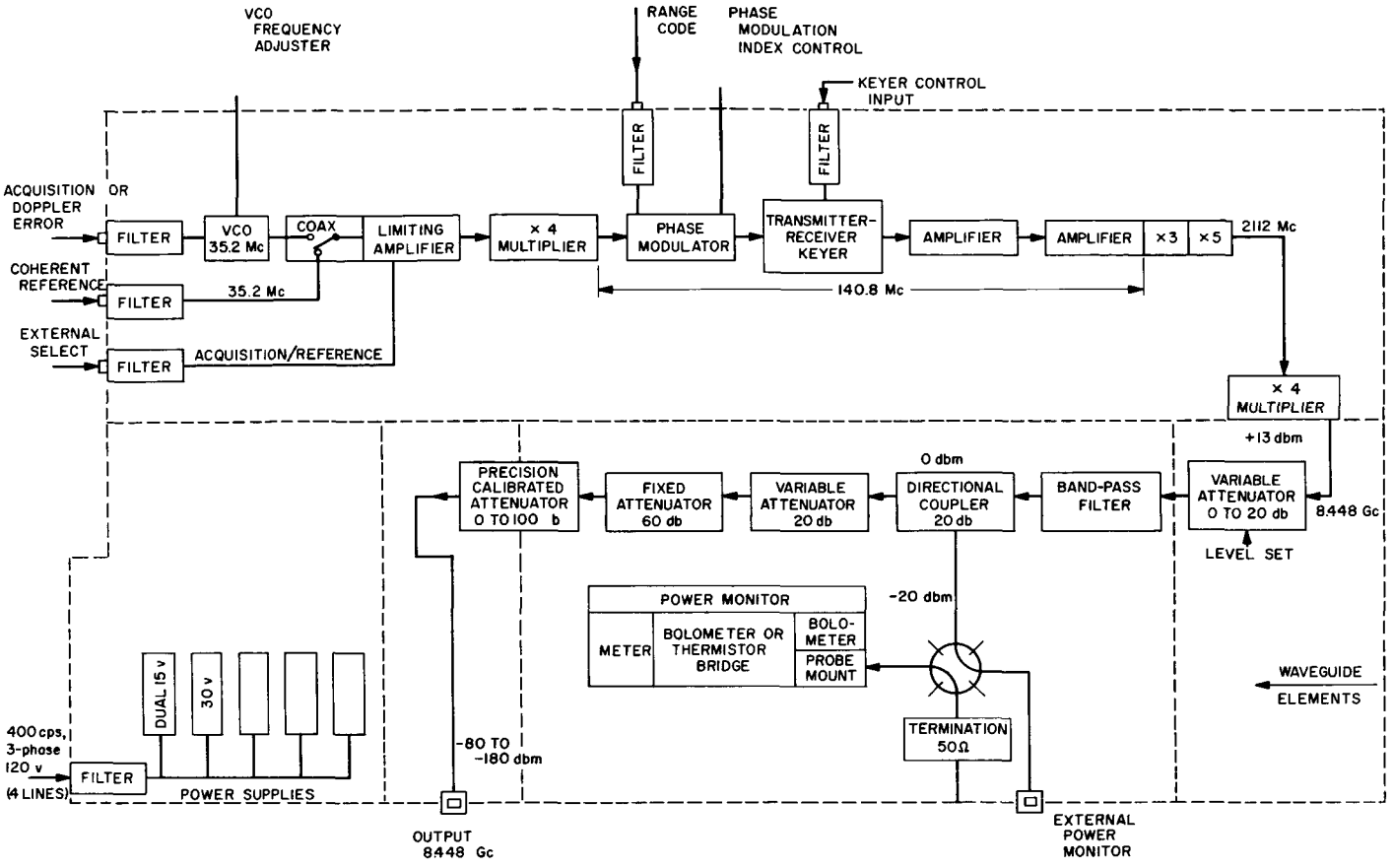


Fig. 41. 8.448-Gc standard signal generator

35.2 Mc which is multiplied by a solid-state ×4 stage to 140.8 Mc. At this frequency, phase modulation is performed by means of a newly developed digital-type, bistate device producing a plus and a minus phase shift, adjustable from ±10 to ±90 deg. Following the phase modulator is a keyer, which functions as an *on–off* switch, as used for keying the transmitter during the transmit–receive cycle.

The keyer is followed by an amplifier stage to achieve the signal level appropriate for operation of the ×15 multiplier stage, next in line. The multiplier unit consists of a limiting amplifier, a ×3 and a ×5 element. The output frequency at this point is 2112 Mc.

Following this is a ×4 multiplier stage, the output of which is the final frequency of 8.448 Gc and this constitutes the point of transition to waveguide elements in the physical configuration. It should be pointed out that other signal generators designed at JPL have been at S-band and so were coaxial devices throughout. This unit is at X-band in the critical parts where level set, attenuation, and power measurement occur so waveguide must be used posing a new series of problems.

An adjustable attenuator is next in line to achieve a standard monitoring level. The signal is then fed through a band-pass filter, designed to pass the fundamental output frequency and its side band components only, and through a directional coupler which divides the signal between the output path and the monitoring circuitry.

The output consists of an adjustable attenuator and a precision-calibrated continuously variable attenuator. Use of a series step attenuator to facilitate accomplishment of the required range (−80 to −180 dbm) is unfeasible, because of the requirement for an uninterrupted signal during variation of attenuation setting. (A signal interruption would result in system loss of lock.)

The monitoring circuit contains a waveguide switch for selection of internal or external power monitor. The internal monitoring system comprises a bolometer (barretter or thermistor), probe mount, bolometer bridge circuitry and meter (with standard reference level mark).

E. Telemetry System Development

1. Design of Punctured Cyclic Coder-Decoder

a. Introduction. The punctured cyclic coder, introduced by Solomon and Stiffler in Ref. 32, is a device for encoding and decoding a fixed number k of binary data symbols into any of the nontrivial (n, k) $(n \leq 2^k - 1)$ linear codes which exist for that k. Thus, one machine has the capability of using the code which best satisfies the daily varying physical constraints of a particular communication system. The code can be readily changed as those constraints change. This feature is useful in time-varying links such as interstation teletype links (Ref. 33). The encoder–decoder is only slightly more complex than one designed for the $(2^k - 1, k)$ code alone. This article discusses a design of such a coder–decoder for $k = 6$ information bits. The machine will be built using the new line of digital circuit modules being developed by JPL (page 123 of this report).

b. Background. The basic idea of this coder is to have an encoding and decoding procedure for a parent $(2^k - 1, k)$ maximal length shift register code, which procedure is modified slightly for codes of smaller length n by a so-called puncturing program which deletes, or punctures, fixed check bits of the parent code.

To encode, a shift register acts upon k information bits and generates words of length $2^k - 1$, all of which have 2^{k-1} *ones* (except for the all-*zero* word). For codes of length n smaller than $2^k - 1$, a "puncture program" with *ones* in each of the coordinates to be deleted, and with *zeros* elsewhere, circulates synchronously with the shift register sequence. *Zeros* of the puncture sequence are used to control a high-frequency clock which shifts undesired coordinates away before they are transmitted.

The decoding procedure will now be reviewed. Let a be the received word. For b any fixed non-*zero* code word, let $T^i b$ denote the ith cyclic shift of b, $0 \leq i \leq 2^k - 2$. The machine then computes the weight (number of *ones*) $w(T^i b \oplus a)$ of $T^i b \oplus a$ as i varies from 0 to $2^k - 2$, and also computes the weight of a, $W(a)$. The machine then chooses the word $T^i b \oplus a$ with the minimum weight as the transmitted word, unless $W(a)$ itself is the lowest, in which case the all-*zero* word is assumed transmitted. For punctured codes of length $n < 2^k - 1$, the computation of $W(T^i b \oplus a)$ is done only over the unpunctured positions.

c. System design of encoder. The encoder consists of the following basic functional blocks: (1) data source simulator, (2) K-register, (3) control counter, (4) puncture sequence program, (5) output control, and (6) clock system. The system block diagram, Fig. 42, shows the connections between the various blocks.

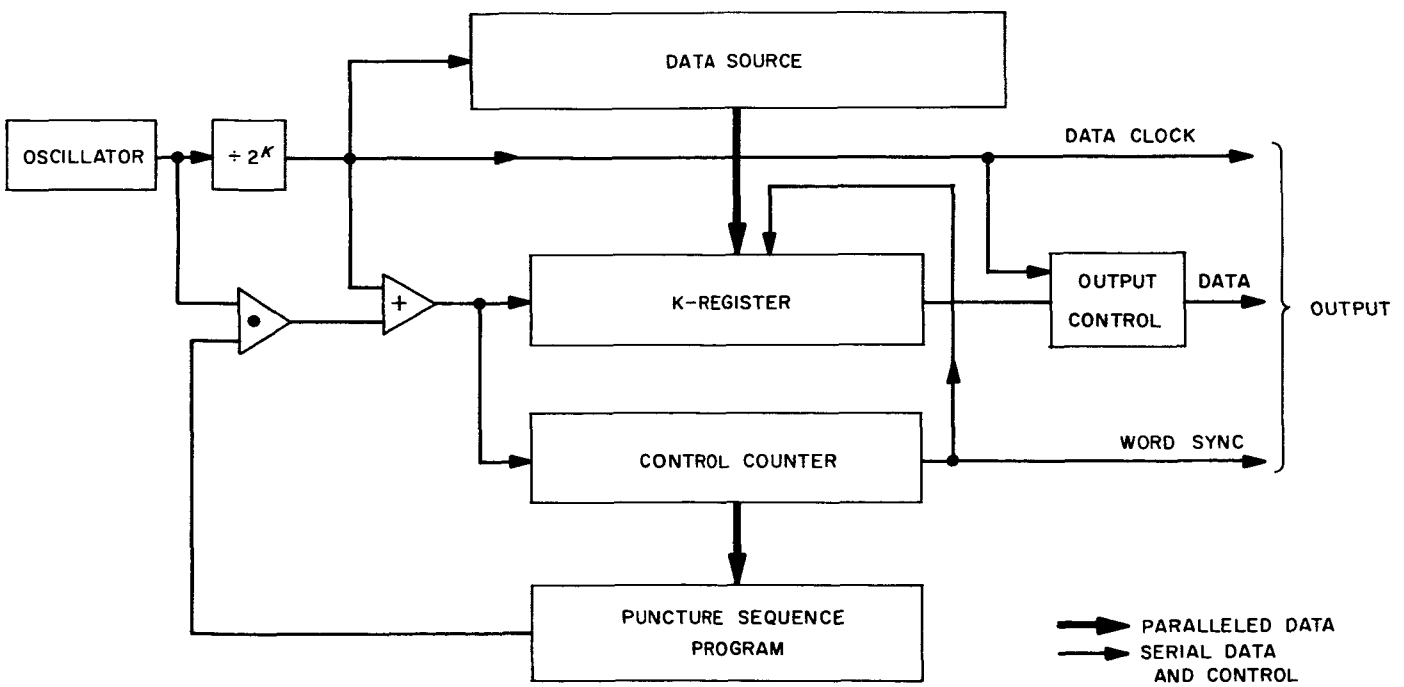


Fig. 42. Punctured cyclic encoder

The data source simulator consists of a maximum length shift register generator as described previously. A block of k symbols is entered serially or in parallel to the data word register, called the K-register.

The K-register contains k bits and is connected as a linear recurring sequence generator of length $2^k - 1$. Upon transfer of a data word from the data source simulator to the K-register (in a nonpunctured sequence), the k-symbol data word is transmitted, using $2^k - 1$ symbols. Upon completion of transmitting one data word, a second data word is transferred and then transmitted. The completion of a data word transmittal is detected by the control counter.

The control counter consists of a k-bit binary counter counting $2^k - 1$ positions. A cycle output from the control counter constitutes the transfer command for data from the data source simulator to be transferred to the K-register. The control counter operates off the same input as the serial input to the K-register. The control counter also controls the puncture sequence program. The cycle output is also transmitted as a word sync signal.

The puncture sequence program consists of an X-Y scanning matrix connected to scan a program pin board. The output is in the form of a series of $2^k - 1$ bits and is used to control a high-frequency service clock that is one term in an *or*-function, the output of which feeds both the K-register and the control counter. The other term is the data clock.

The puncturing operation will now be described. The code word that is the output of the K-register and the puncture sequence program are of the same length $2^k - 1$, and have the same timing. For sake of explanation, the two can be looked upon as two side-by-side shift registers of the same length, operating on the same shift clock. One register then contains the code word, whereas the other contains the puncture sequence program. The two registers are shifted in parallel at all times. The shift pulse is normally the data clock. However, if a *one* is the output of the puncture sequence program register, a high frequency (on the order of 2^k times the data clock) is gated in as a shift clock. The high-frequency shift is maintained for any series of *ones*. Since the high-frequency shift is controlled by the output of the shift operation, it is evident that if a *zero* is an output, the high frequency is inhibited until another *one* is the output, as a result of a shift executed by the next pulse from the regular data clock. During this rapid shift, which in effect constitutes the puncturing, no change in the output data occurs. The output data is controlled by a separate output control.

The output control unit simply consists of one flip-flop. The enable inputs to the flip-flop are the outputs from the K-register, and the trigger inputs are derived from the data clock. In this manner, the punctured bits will not be recorded at the output.

The clock system consists of a system clock generator. This clock generator furnishes the shift frequency for the rapid shift during the puncturing process. A frequency divider that divides the basic system clock by 2^k is used to provide the data clock. Clock facilities are thus included for puncturing of all symbols in a code word at once. That is to say, $2^k - 1$ bits can be shifted at the system clock rate within one data clock period.

d. System design of decoder. The purpose of the punctured systematic cyclic encoder–decoder system is not so much to demonstrate the mechanics of data transmission and receiving, data reconstruction, bit clock generation, word synchronization, etc., but, much more, to demonstrate an encoding and decoding scheme. Thus, the input to the decoder, the data clock, and the word sync derived from the encoder through closed circuits. The data format, however, resembles that of a regular transmission: data entered to the decoder serially. The decoder consists of these functional blocks as shown in the decoder block diagram, Fig. 43:

(1) Input: input multiplexer, input registers, and program counter.

(2) Calculation of weights and word selection: word correlation comparator, word correlation counter, previous-low correlation register, comparator, and *zero* word control.

(3) Calculation of $(T^i h)_l$: Program counter, K-register, vector *anding*, and modulo 2 circuit for six variables.

Input. The input multiplexer is used to energize one of the input controls, and to allow the incoming word to be loaded serially into one of the input registers. The multiplex control consists of a single flip-flop which complements on each word sync. Decoding of one word will then take place while the next word is being loaded into the opposite input register. The actual steering of the incoming signal into the appropriate register will be accomplished by the input controls. These two identical circuits contain a gating structure, which uses the multiplexer output to determine whether the input register

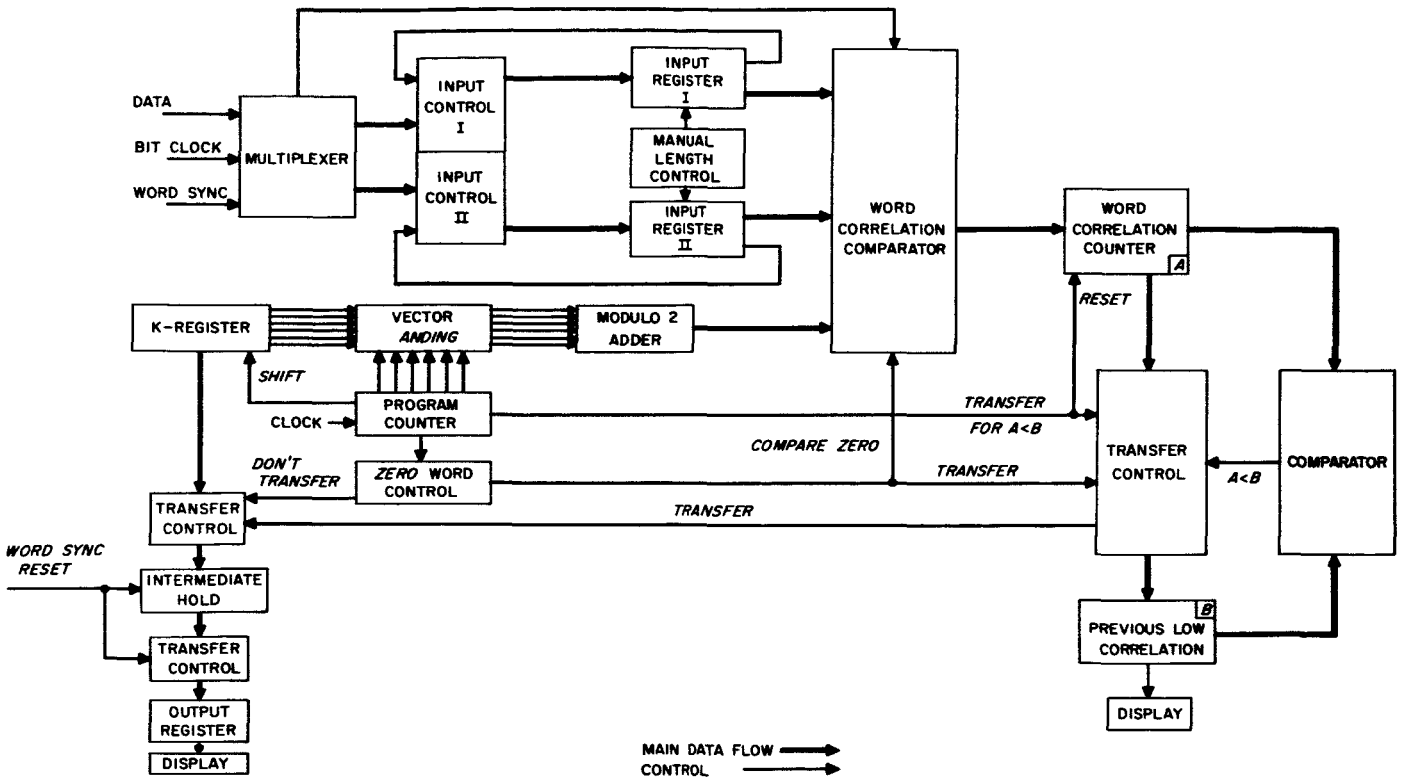


Fig. 43. Punctured cyclic decoder

receives the new data word or receives the output of the input register's own last stage. The input registers are connected as shift registers, each with 63 stages. While one of these registers is accepting the input data, its clock is the data clock. But when the register is used for decoding, its clock is changed to high-frequency service clock by the input control. When the data word was less than 63 symbols long due to puncturing, the length of both input registers is changed to agree with the length of the word. This change is effected by the manual length control that operates in binary increments.

Calculation of weights, and word selection. The theory of the decoding process outlined above dictates the calculation of the weight $w(T^i b \oplus a)$. The most difficult portion of this calculation is the generation of $T^i b$, and this portion will be described separately here. Assuming for the moment then that $T^i b$ is available, the process is performed as follows. The weight calculation is performed serially by comparing one bit, a_l, of the word a with one bit $T^i b_l$ of $T^i b$ in the word correlation comparator. This comparator is a circuit which performs the modulo 2 sum of its inputs. Each disagreement between the corresponding bits is then counted in the word correlation counter as l varies from 0 to n, the length of the word. At the completion of the comparison for $T^i b$, a recycling signal from the program counter signals a comparison between the weight just calculated and the weight of the previous low correlation. This previous low is stored in the previous low correlation (PLC) register. If this new weight is, in fact, lower than the previous low, it is transferred to this PLC register. Then the information bits (the first six bits) of $T^i b$ are transferred to an intermediate hold register. Enough time has been allotted for $w(T^i b \oplus a)$ to be calculated for all i before the next word has been completely received. When the next word is ready to be decoded, the word sync transfers the contents of the intermediate hold register to the output register.

The all-*zero* word unfortunately presents a special case in decoding since the coded word is again all *zeros*. It is found best to treat this special case by adding a flip-flop to the program counter called the *zero* word control. This control is caused to signal a slight modification in the machine to accommodate the all-*zero* comparison. Namely, the *zero* word flip-flop is set to the *zero* state at word sync, and remains in this state until the program counter delivers a recycling signal, indicating the completion of the calculation of $w(0 \oplus a) = w(a)$. The modifications to the machine during this time are the additions of the following signals: a *compare zero* signal delivered to the

word correlation comparator, a *transfer* signal which allows the word correlation counter to transfer to the PLC register (thus resetting this register), and a *don't transfer* signal which maintains the intermediate hold register in its reset (all-*zero*) state. Thus, the PLC register will always start the cycle at the weight of the received word. If it should turn out that this weight is the lowest correlation achieved, the intermediate hold register will never receive another signal and so will indeed indicate the correct output.

Calculation of $(T^ib)_l$. If there were no puncturing involved, the calculation of T^ib would be very simple. A shift register yielding the maximal length sequence could run along in sync with the received word and generate (T^ib), as l varies from 0 to $2^k - 1$. A shift of this register with respect to the received word would then allow i to vary from 0 to $2^k - 1$, and thus finish the decoding process. When puncturing is involved, however, this technique has to be changed. It would be possible to use a decoding scheme similar to the puncturing of the encoder, i.e., to shift the punctured bits of the maximal length sequence away while holding the data word fixed. This method, while economical from the hardware point of view, is extravagant in the use of time. With this extravagant method, the time used to decode a punctured word is exactly the same as an unpunctured word. The method to be used in this device uses hardware rather than time to calculate the $(T^ib)_l$. This tradeoff results in a decoding time which is directly proportional to the length of the punctured word.

When a code word a of length $n < 2^k - 1$ is circulating in the input register, it is necessary to match the ith component of a with the $\phi(i)$th component of T^ib, where $\phi(i)$ is a function which will be known for each puncturing. For example, in a certain (60, 6) code, the 7th, 8th and 13th components of the (63, 6) code have been punctured so that the $i = 7$th component of the punctured word is the $\phi(i) = 9$th component of the unpunctured code word T^ib. This same reasoning applies to every word in the dictionary. That is, no matter what the puncturing is, there are still $2^k - 1 = 63$ words in the dictionary, and each is simply the same mapping of the (63, 6) dictionary onto the $(n, 6)$ dictionary by a deletion of exactly the same coordinates of the parent code word.

The parent (63, 6) code is generated with a 6-bit K-register with a modulo 2 feedback of its last two positions. Thus, the recursion relation for terms in this sequence is $b_n = b_{n-5} \oplus b_{n-6}$ (for example, $b_{12} = b_7 \oplus b_6$). But since $b_7 = b_2 \oplus b_1$ and $b_6 = b_1 \oplus b_0$, the recursion implies $b_{12} = b_7 \oplus b_6 = b_2 \oplus b_1 \oplus b_1 \oplus b_0 = b_2 \oplus b_0$. This last step is possible due to the fact that $b_1 \oplus b_1 = 0$. Similarly, every term in the sequence can be written as a linear combination of the six generators b_0 through b_5. Thus

$$b_n = c_0^{(n)}b_0 \oplus c_1^{(n)}b_1 \oplus c_2^{(n)}b_2 \oplus c_3^{(n)}b_3 \oplus c_4^{(n)}b_4 \oplus c_5^{(n)}b_5 = C^{(n)} \cdot B$$

say, for all n and some set of constant c_i. The conclusion is that any b_n can be calculated using the same set of six generators b_i, $0 \leq i \leq 5$, *anding* them with the proper $c_i^{(n)}$, and then sending the result to a circuit which generates the modulo 2 sum of six variables.

These $c_i^{(n)}$'s are very easy to calculate and are listed in Table 6. For it can be proved that the $c_i^{(n)}$, i fixed, obey the same recursion formula as do the terms in the original maximal length sequence, i.e.,

$$c_i^{(n)} = c_i^{(n-5)} \oplus c_i^{(n-6)}, \quad 0 \leq i \leq 5.$$

The problem of generating the $\phi(i)$th component of T^ib is now seen to reduce to the problem of generating the set of $C^{[\phi(i)]}$ in the proper order. These will be generated by the program counter, an easily programmed device that will count through any specified sequence of vectors.

Referring to the block diagram of the system (Fig. 43), the program counter will be set for a specific puncturing to count through the proper sequence of $C^{[\phi(i)]}$. Then these values will be *anded*, component by component, with the contents of a K-register in the vector *anding* circuit, and next fed to a circuit which performs the modulo 2 sum of the 6 variables at its input. The output of this circuit then is the $(T^ib)_{\phi(i)}$.

While the $c^{[\phi(i)]}$ are varying, the K-register remains fixed until the program indicates it has finished its cycle. After this completion indication, the K-register shifts once, and the circuit is ready to generate $(T^{i+1}b)_l$ in the proper order. In this manner $(T^ib)_l$ is generated for all $0 \leq i \leq 2^k - 2$ and all l, $0 \leq l \leq n$.

e. Error introduction. Since the system described in this article is to be an advanced engineering system to demonstrate the method and theory involved in the puncturing concept, the aim has been to make it as versatile as possible. The program counter will provide a method to allow the programming of all puncturings, and not just those dictated by some theory. Since puncturings might

Table 6. The $c_i^{(n)}$, $0 \leq i \leq 5$, $0 \leq n \leq 62$

	$c_0^{(n)}$	$c_1^{(n)}$	$c_2^{(n)}$	$c_3^{(n)}$	$c_4^{(n)}$	$c_5^{(n)}$		$c_0^{(n)}$	$c_1^{(n)}$	$c_2^{(n)}$	$c_3^{(n)}$	$c_4^{(n)}$	$c_5^{(n)}$
0	1						32	1			1		
1		1					33		1			1	
2			1				34			1			1
3				1			35	1	1		1		
4					1		36		1	1		1	
5						1	37			1	1		1
6	1	1					38	1	1		1	1	
7		1	1				39		1	1		1	1
8			1	1			40	1	1	1	1		1
9				1	1		41	1		1	1	1	
10					1	1	42		1		1	1	1
11	1	1				1	43	1	1	1		1	1
12	1		1				44	1		1	1		1
13		1		1			45	1			1	1	
14			1		1		46		1			1	1
15				1		1	47	1	1	1			1
16	1	1			1		48	1		1	1		
17		1	1			1	49		1		1	1	
18	1	1	1	1			50			1		1	1
19		1	1	1	1		51	1	1		1		1
20			1	1	1	1	52	1		1		1	
21	1	1		1	1	1	53		1		1		1
22	1		1		1	1	54	1	1	1		1	
23	1			1		1	55		1	1	1		1
24	1				1		56	1	1	1	1	1	
25		1				1	57		1	1	1	1	1
26	1	1	1				58	1	1	1	1	1	1
27		1	1	1			59	1		1	1	1	1
28			1	1	1		60	1			1	1	1
29				1	1	1	61	1				1	1
30	1	1			1	1	62	1					1
31	1		1			1							

be tried for which error-correcting properties are unknown, it has been decided to have a completely variable error-introduction circuit.

The errors will be introduced in the encoder by introducing the modulo 2 sum of the K-register with an error signal, just prior to the output register. The same pinboard used for the puncturing program will be used to introduce errors. For error introduction in one given coordinate of the word, a pin which connects the second and third layers of the pinboard, rather than the first and third, which are used for puncturing, will be inserted. An error signal will be produced thereby, which will invert that bit in the transmitted word. Thus, not only the exact number of errors will be known but their positions also. A later version would use a random pulse generator to introduce the errors automatically.

f. Circuits of special interest. Most of the circuits used in this device are well-known arrangements of *nand*-gates and flip-flops, except perhaps for the comparator, the program counter, and the modulo 2 circuit for six variables. These three will now be explained in more detail.

Comparator. The comparator is the circuit which compares the binary number in the word correlation counter A with the number in the previous low correlation register B. The output of the circuit is an $A < B$ signal, which signals a transfer of the new low correlation. The comparator circuit is shown in Fig. 44, where, for clarity, it has been assumed that A and B are only 4 bits each. (The triangle is the symbol adopted for a *nand*-gate.)

The low level output is the indication that $A < B$. It will be noticed that any one of the four output gates in parallel is capable of pulling the others low, and thus the operation of each is easily understood. The uppermost gate with inputs A_8 and B_8 will go low only if A_8 is *zero*

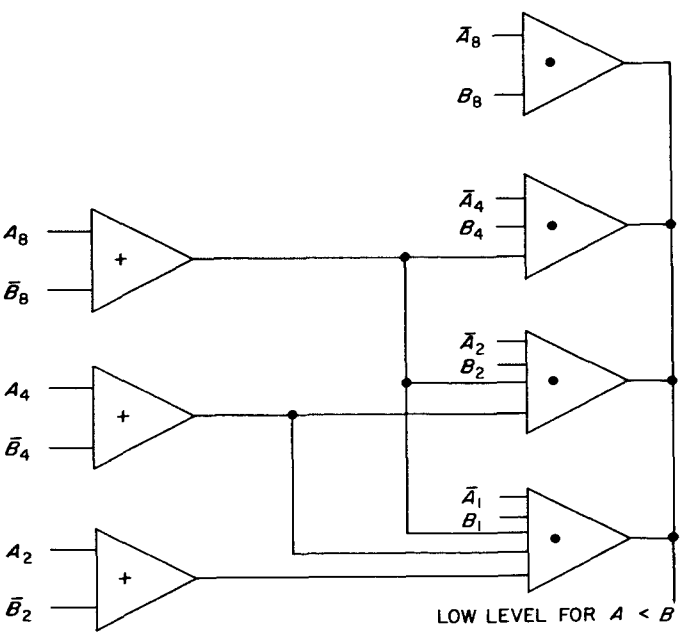


Fig. 44. Comparator circuit

and B_8 is *one*, which means the most significant digit of A is less than that of B and hence the binary A is less than B.

However, if this is not the case, and A is nevertheless still less than B, then one of the other digits of A is less than the corresponding digit of B. One output gate is thus supplied to compare each of the lower order bits of the two numbers to check if $A_i < B_i$. However, we do not wish to examine any one of these possibilities if in actuality $B < A$. For this reason each of the lower order bit gates controlling the output is itself controlled by a check on all the higher order bits, to make sure B is not less than A. The above reasoning leads to a factorization of the $A < B$ function that leads to a very simple two-level circuit using fewer gates than any previously known.

Program counter. The program counter is a device which can be programmed to count through any sequence of 6-digit binary numbers. Six flip-flops have their output completely decoded, using a standard decoding matrix (Fig. 45). So, for any particular setting of the flip-flops, only one of the 64 outputs A will be energized. Then, using a patch cord arrangement between terminals of A and those of B, the feedback to the flip-flop enable terms is adjusted by means of an encoding matrix so that the next state will be that number of B which is energized. For example, if the present binary number in the counter is $(000001)_2 = 1$ and terminal $1A$ is connected to terminal $63B$, the counter will immediately go to $(111111)_2 = 63$ on receipt of the next clock pulse. Thus, a closed loop of patch cords will enable the counter to go through any sequence of binary numbers of any length up to 64. The sequence can be synchronized through collector reset of the counter flip-flops.

Six-variable modulo 2 sum. Fig. 46 shows the minimum circuit for forming the modulo 2 sum of six variables. The idea is to break the six variables into two groups of three variables, form the modulo 2 sum of each group and then to take the modulo 2 sum of these results.

g. System capabilities. A partial listing of the codes which can be encoded and decoded by this machine is

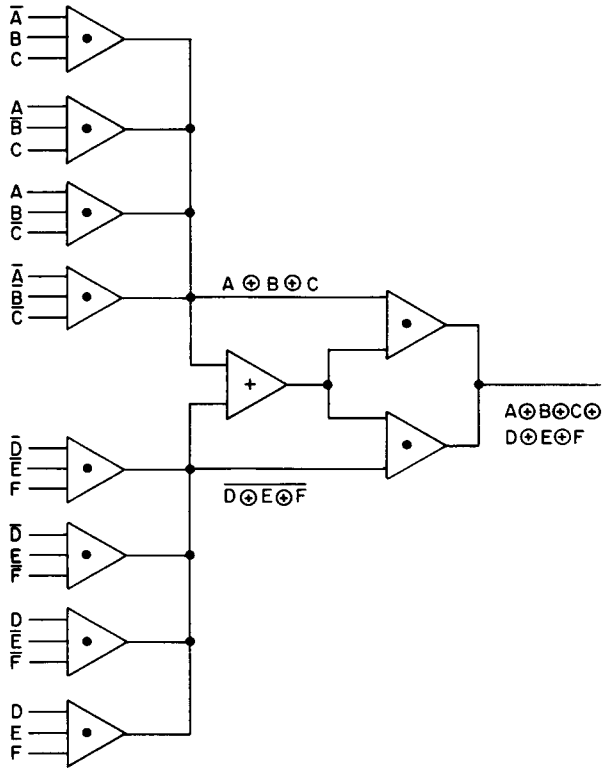


Fig. 46. Modulo 2 sum of six variables

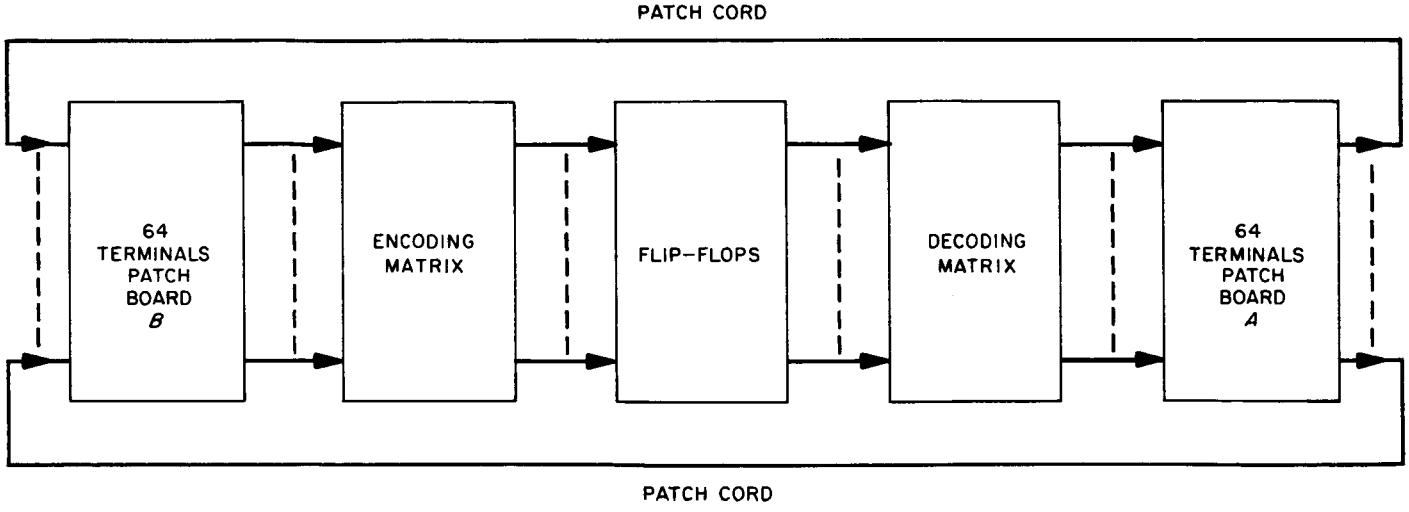


Fig. 45. Program counter

Table 7. Some codes available

n	d	e	Punctured coordinates
63	32	15	None
60	30	14	7, 8, 13
56	28	13	7, 8, 9, 13, 14, 19, 33
53	26	12	7, 8, 9, 10, 11, 13, 14, 16, 19, 33
48	27	11	7, 8, 9, 10, 13, 14, 15, 19, 20, 25, 33, 34, 39, 42, 55
45	22	10	7–15, 17, 19, 20, 25, 33, 34, 39, 42, 55
42	20	9	5–15, 17, 19, 20, 25, 31, 33, 34, 39, 42, 55
38	18	8	13, 14, 15, 16, 19, 20, 21, 23, 25, 26, 31, 33, 34, 35, 39, 40, 42, 43, 45, 48, 52, 55, 56, 59, 61
32	16	7	7, 8, 9, 10, 11, 13, 14, 15, 16, 19, 20, 21, 23, 25, 26, 31, 33, 34, 35, 39, 40, 42, 43, 45, 48, 52, 55, 56, 59, 61, 63

shown in Table 7 which gives the length of the code for the constant number of generators $k = 6$. Also given are the minimum distance d, the error-correcting capability e, and the coordinates that are to be punctured to generate the code. It should be pointed out that the punctured coordinates represent only one possible set, and any cyclic shift of these numbers is also a valid puncturing.

All of these codes can be coded and decoded at a machine rate of 2 Mc. This results in maximum symbol rate of 2 Mc/64 $\approx$ 30 kc. For the (63, 6) code, this yields $6/63 \times 30$ kc, or 2.86 kc in information bits, which is considered a moderate rate. However, for a (7, 6) code the bit rate is $6/7 \times 30$ kc, or the rather high rate of 25.7 kc.

2. Design of a Quantile System for Data Compression of Space Telemetry

a. Summary. The theory of data compression by quantiles was first introduced by Easterling, Eisenberger, and Posner in Ref. 34, and further developed in Ref. 35. This system allows the reconstruction of histograms, previously generated on board a spacecraft, from the values of only a few *sample quantiles*, or percentage points, of the histogram. Large data compression ratios, coupled with high statistical efficiencies, were found in Ref. 35. This article discusses the actual design of an engineering prototype of a digital machine for computing quantiles on board a spacecraft. The machine will be built using the new line of digital circuit modules currently under development in the Communications System Research Section (Ref. 36).

b. Statistical review. Statistical data consists of numerical observations resulting from the performance of experiments for which the outcomes cannot be predicted, except in terms of probability of occurrence. The underlying assumption in statistical theory is that the observations obey a probability law which may or may not be known *a priori*. Each observation is said to be a *sample value* taken from a population with a *probability distribution* characterized by a *distribution function* $G(x)$, $G(x)$ = Probability $(X \leq x)$, where X denotes a random quantity or *random variable*. The probability law associated with X (or with the given *population*) can be expressed entirely by $G(x)$.

If $G(x)$ were completely known, it would not be necessary to perform experiments in order to form statistical conclusions about the population with which $G(x)$ is associated. Hence, the fact that experiments are indeed performed implies that $G(x)$ is at best imperfectly known. The sample values are then used to estimate those characteristics of $G(x)$ which are of interest but unknown. Since the uncertainty of an estimate (usually expressed in terms of the variance of the estimate) in general decreases with increasing sample size, a large sample size is desirable from this viewpoint.

In certain circumstances, however, the locality where the experiments are performed and the results recorded does not coincide with the locality where the statistical computations are performed. The sample data must then be transmitted through a communications channel from the point of origin to the processing center. If the rate of transmission is not of critical importance, this procedure presents no more of a problem for a large number of samples than for a small number. If, on the other hand, many experiments are being performed simultaneously and, in addition, the same communication channel is used to transmit the sample values of each experiment, there is a limit to the total number of observations that can be sent in a given time. This limits the number of experiments which can be performed in the given time for given sample sizes. The situation on board a space probe relative to the number of experiments that can be performed falls precisely into this category. This situation accounts for the desire to achieve a significant amount of data compression with a minimum amount of information loss from the received data. One way of effecting data compression is by transmitting a small number of sample

quantiles, instead of all the sample values, and extracting the desired statistical information from these quantiles.

Some of the definitions and results from Ref. 35 will now be reviewed. Let $G(x)$ be a probability distribution function. In the case of empirical data, $G(x)$ is defined as the fraction of experimental outcomes below x. Then the quantile of order p, z_p, of the distribution $G(x)$ is defined as the largest value of x satisfying $G(x) \leq p$. In the case of which G is continuous, z_p is the value below which X lies with probability p. For the discrete case, z_p is the largest value just before the fraction of samples jumps above p. This definition is illustrated in Fig. 47.

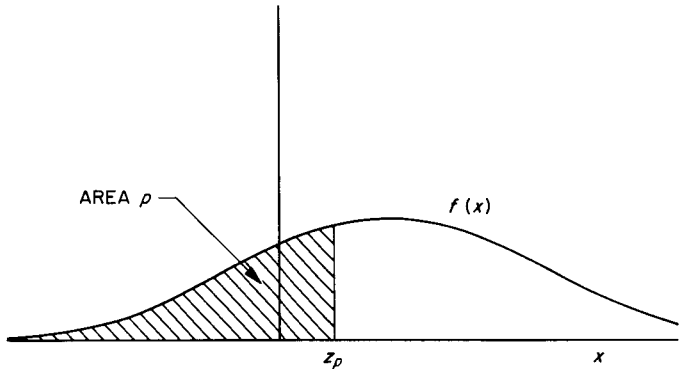


Fig. 47. Definition of quantile

Think of $G_1(x)$ as a parent distribution about which information is desired. We obtain an experimental distribution or histogram $G(x)$, and obtain a certain number of quantiles ζ_p of the experimental distribution. We then are in a position to make statistical inferences about the original distribution $G_1(x)$. Let us look into this matter further.

The sample quantiles, being random quantities, have probability distributions of their own, with the useful property in most cases of interest that as n approaches infinity the joint distribution of any number of quantiles approaches a known multivariate normal distribution. Thus, for a sufficiently large sample size, if the limiting normal distribution of the sample quantiles is assumed when a statistical analysis is based on quantile values, the error involved in so doing will be small. Since experiments aboard a space probe often involve large numbers of observations (a sample size of 1000 is not uncommon) the assumption of normality is amply justified. The importance of being able to assume the normality of the distribution of the sample quantiles lies in the fact that normal distributions are amenable to many types of statistical analyses.

Estimates of the parameters of the distribution associated with a population and the results of tests of statistical hypotheses are two of the important types of statistical information desired from experiments performed on board a space probe. Using a small number of quantiles to obtain this information means that only a few numbers need be transmitted to Earth instead of all the sample values, resulting in a high data compression ratio R. This compression would be of little value, however, if the reliability of the information thus acquired were proportional to the ratio of the number of quantiles used to the total number of observations. That this proportionality is not the case accounts for the advocacy of the use of quantiles.

For example, if the distribution of the parent population is normally distributed with unknown mean μ and standard deviation σ, estimators for μ and σ using simple linear combinations of the sample quantiles have been constructed. The case considered in Ref. 35 used from 2 to 20 quantiles, chosen optimally. The efficiencies range from 0.81 to 0.99 in the case of μ and from 0.65 to 0.98 in the case of σ (the efficiency of an estimate is defined as the ratio of the variance of the best estimate using all the sample values to the variance of the estimate using quantiles). Furthermore, the efficiencies of the estimates using quantiles are relatively insensitive to deviations of the parent population from normality. In addition, tests of statistical hypotheses have been devised using a relatively small number of quantiles, each test with a reliability (power) which compares favorably with that of a test using the entire sample.

Thus, it can be seen that by using quantiles in an optimal manner to obtain statistical information, not only can a significant amount of data compression be achieved, but the reduction in uncertainty which accompanies a large sample size is also retained.

c. Compression ratios. Here the data-compression ratio attained with the use of quantiles is estimated; it has already been observed that a high statistical efficiency is attained with the use of quantiles. The discussion here shall assume a full sample size of 1024 and the use of four quantiles.

In the system to be discussed later in this article, the 1024 samples are particle counts from 1024 sec. It is assumed that not more than 255 particles arrive in any second; this means that an 8-bit word is required to specify the number of particles per second. Thus, 8192 bits are required every 1024 sec in the uncompressed, or raw data, system.

Let us look more closely at the quantile system so that we can compare it with the raw data system fairly. A typical histogram obtained is shown in Fig. 48, using quantiles of order 0.067, 0.291, 0.709, and 0.933; 1024 sec are assumed. The first item to note is that the quantiles should be transmitted with somewhat more signal-to-noise than used for the raw data. An error in the raw data is not serious, since such errors averaged out with 1023 other data points. But an error in a quantile value causes all estimates to be far off. Let us assume that we have a coherent telemetry system, with raw data bit error probability of 10^{-2}, which is as high as one would ever accept. We might suppose that an error probability in the sample quantiles of 10^{-5} would be as good or better. But it can be shown that a bit error probability of 10^{-2} drops to 0.16×10^{-5} by doubling the signal-to-noise ratio (Ref. 37). Thus, doubling the signal-to-noise ratio, or, equivalently, doubling the time per bit with power fixed, takes care of the noise sensitivity of the estimates. So we remember that one bit in the quantile system is to be counted as *two* bits for purposes of comparison with the raw data system.

Each quantile takes 8 of these double bits, since each quantile is an integer between 0 and 255. However, we must transmit more than just the quantiles because many of the histogram slots hold a large integer and the quantiles will not often be reached exactly at a division of

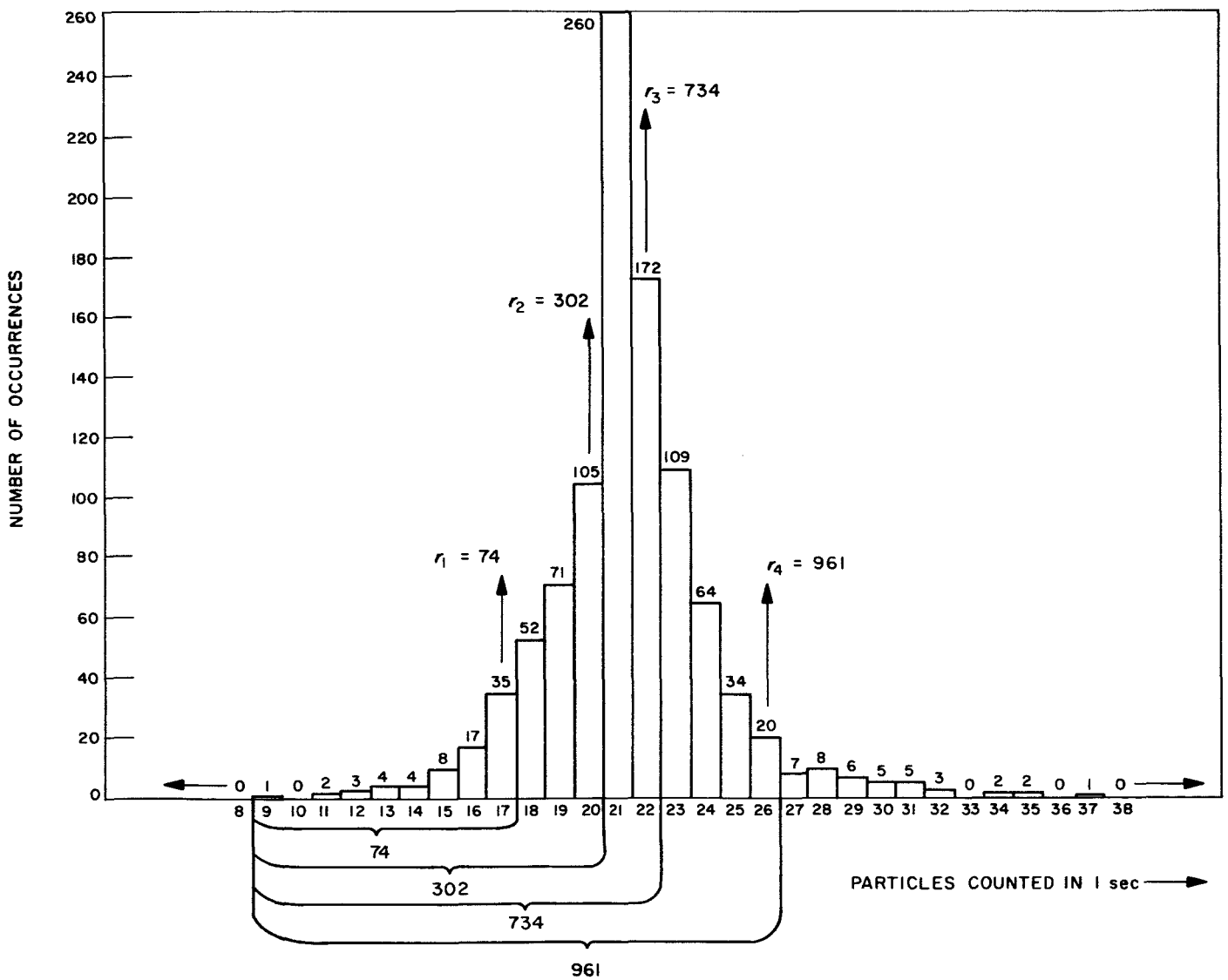


Fig. 48. Typical histogram

histogram slots. Instead, the addition of the contents of one more slot would jump over the sample quantile. For example, if we are looking for the 0.067 sample quantile from 1024 observations, we want the 69th observation in size. But there would usually be a tie—many observations would be the same. For example, slots 15 and below might cover 61 sec, and slot 16 might contain 14 sec. The 0.067 quantile would be the 16 slot, but we should also know the actual number of seconds in that slot in order to get a still clearer picture of the sample distribution. Using a fixed word length for this information requires 10 bits. Let them again be double bits (even though low error probability is not as vital at this point). Thus, this histogram information takes 10 double bits per quantile.

So, for each of the 4 quantiles we require 8 double bits for the quantiles themselves, and 10 double bits for the histogram information. Therefore, in single bits, $(8 + 10) \times 2 = 36$ bits are required per quantile. Since there are 4 quantiles, 144 bits are required in the quantile system. Remembering that these data are transmitted only once every 1024 sec, we see that 144 bits/1024 sec are required by the quantile system.

Since in the raw data system 8192 bits are required every 1024 sec, the data compression ratio obtained with the use of the quantile system is 8192/144, or 57.9 to 1. However, remember that the use of 4 quantiles gives statistical efficiencies of say 80% for most purposes. By increasing the sample size with the quantile system by a factor of 1.25, we can cut the variances obtained with the quantile system by a factor of $1/1.25 = 0.8$. Relative to the original raw data system with 1024 sec (instead of 1280), we now have 100% efficiency with the quantile system.

However, the number of bits in the quantile system has been increased by ¼, from 144 to 180. Thus, to obtain this 100% efficiency, we need 180 bits, as opposed to 8192 bits. (Since this experiment is presumably time-sharing the channel with others, the possibility does exist of using 1280 sec instead of 1024 if the quantile system is used.) The data compression ratio is thus 45.5 to 1 at 100% efficiency.

In short, by the use of the quantile system in a typical case, we can arrange to get estimates with quantiles just as good as those we get with raw data. And less than 1/45 as much channel is used. In subsection (*e*) of this article we exhibit a design for a quantile system which demonstrates the simplicity of the equipment necessary on board the spacecraft. Thus, this high compression is actually achievable in space telemetry.

d. Functions performed by quantile system. It is evident from the definition of sample quantile that no arithmetic unit is needed on board the spacecraft to obtain the quantiles from the raw data. It is this simplicity of the compression equipment which makes the quantile system feasible for flight hardware. All the arithmetic manipulations with the data necessary to make inferences about the parent distribution take place on Earth after reception.

Let us first indicate the kind of operations that must be performed on the raw data to obtain a given number of quantiles of given orders. To be specific, we think of a particle-counting experiment of the following type: Particles arrive at the spacecraft, and the number arriving in 1 sec is counted. This number is the input raw data; 1024 sec of count are obtained. It is assumed in building the counter that not more than 255 counts arrive in any second. (Overflows of the counter will cause the fundamental sampling time to decrease until the input ratio is accommodated, in the design presented here.) At the end of 1024 sec, we have 1024 numbers which are the number of counts in each of the 1024 sec.

The four quantiles for $p = 0.067, 0.291, 0.709, 0.933$, are used, which are the four quantiles for estimating the mean and variance of a parent normal distribution, optimum with respect to minimizing the sum of the variances of the estimate of the mean and standard deviation of the parent normal. The following four numbers are to be found: ζ_1, the smallest count such that $r_1 = 69$ or more of the 1024 sec had at least that count; ζ_2, the same for $r_2 = 298$; ζ_3 for 717 and ζ_4 for 955. As discussed earlier, we also want to know the exact number of seconds that had the count in question, since the exact number is ordinarily greater than the corresponding r_i. Now by assumption, there are only 256 possible counts for any second, so the histogram has 256 slots. We must first assign the count in each second to its proper histogram slot. Then, after counting and assigning for 1024 sec, the quantiles are found. Namely, the histogram slots are to be emptied one by one, starting with the *zero* slot, until r_1 is equalled or exceeded. Furthermore, the total number of seconds used when this first event occurs is to be recorded. Then the emptying continues until r_2, r_3, r_4 are reached. After the quantiles are found, together with their actual values, these are sent to telemetry for transmission to Earth. As will be observed, no arithmetic is done on board the spacecraft.

e. Design of an advanced engineering quantile system. The previous discussion suggests the design of a quantile system. However, an advanced engineering version should have more outputs available than a flight model would, since a demonstration of the quantile system should make available the entire histogram. But the extra output portion will be separated both in the discussion and in the block diagram.

Fig. 49 is a block diagram of the quantile system being built. The various blocks and their operations are discussed here. A quantiler that generates the quantiles for a total of 1024 samples with a sample range of 0–255 is considered. In a quantiler used for a total of 1024 samples each within a spread of 255, only 1280 storage elements (or bits) are needed: 1024 elements represent the actual samples and the 256 elements distinguish the number of samples of each size.

In this quantiler, a 1280-bit circulating delay line is used as the memory. At all times the line contains 256 markers and 1024 spaces. The spaces between two markers represent the number of samples of the size that is indicated by the order of the markers. (Actually, with 256 markers, only 255 different sizes can be registered: each size requires two markers, and the first and the last marker are not always the same.) Two outstanding features of the quantiler are:

Automatic synchronization. The synchronization circuits not only control the initial loading of the markers, but they also realign the markers at the end of such sampling period. At any time, if the marker-to-space balance is disturbed, the balance is immediately restored.

Automatic control of the sampling rate depending on the data rate. This feature can be considered a secondary data compression function. With each change of the sampling rate the markers on the memory line are realigned. No extra data need be transmitted to indicate the sampling rate, since this information is inherent in the rate at which the quantiles are transmitted. These matters will be discussed in more detail.

The block diagram shows the following functional blocks: (A) sampling counter, (B) sample distributor, (C) sample hold register, (D) address register, (E) comparator between C and D, (F) histogram serial memory, (G) cumulator, (H) quantile detector, and (I) central control. The functional blocks listed, together with their

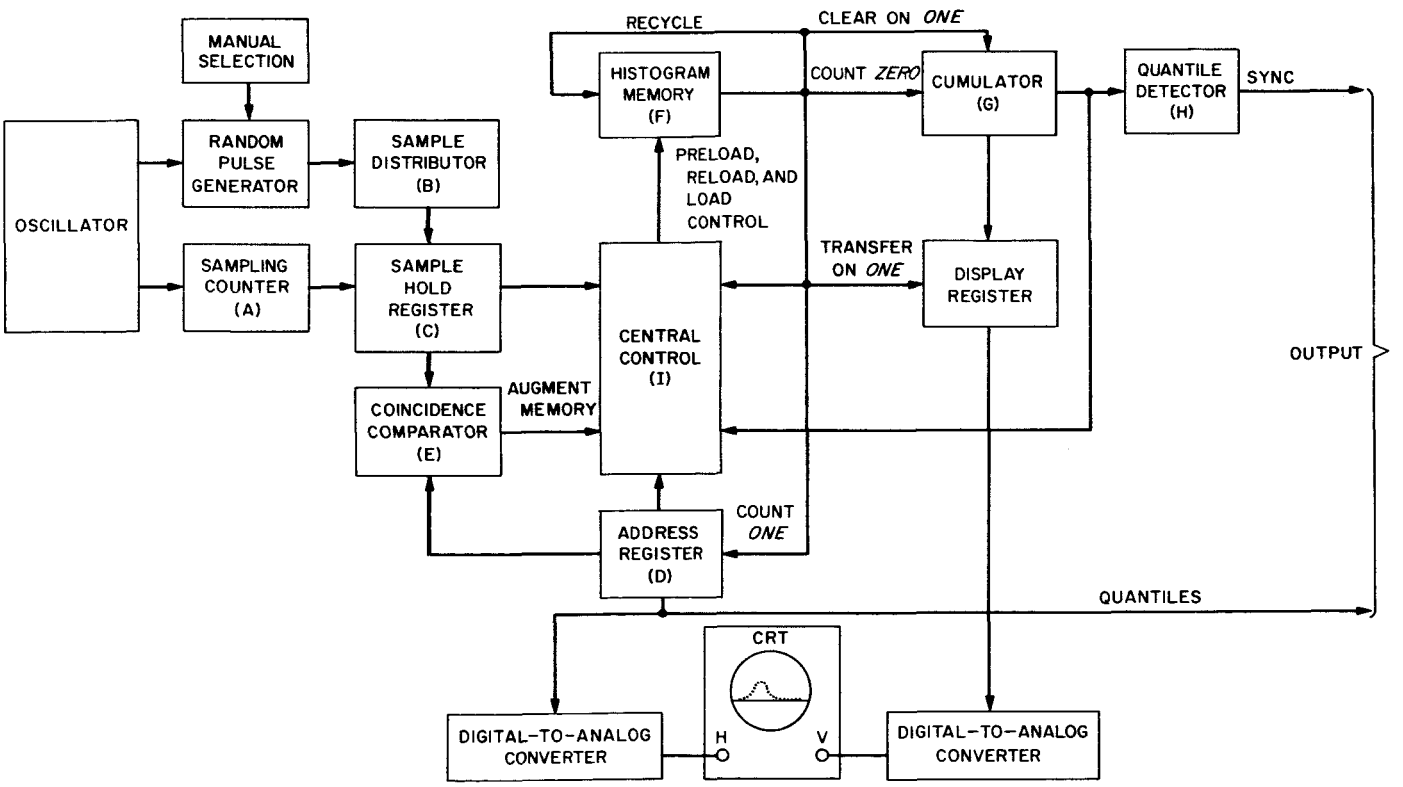


Fig. 49. Quantiler, data source, and display

interconnection, will be discussed briefly. [Blocks shown in Fig. 49 but not listed contain functions necessary for demonstration purposes but not necessary in a flight model. These functions are a data input (see section 3 of this article), and auxiliary display functions. These extra blocks will be discussed later. Also needed would be some arithmetic-computing unit to do the same Earth-based calculations that would be done with quantiles received from a spacecraft. Outputs will be available to allow a general-purpose computer to be used as ground support equipment in demonstrations.]

(A) The sampling counter is a simple frequency divider that provides a constant sampling rate compatible with the average incoming data rate. With significant changes in the average data rate, different outputs from the sampling counter are used. The automatic selection of outputs is described in (I), central control.

(B) The sample distributor is another simple data pulse counter. It is reset at each output from the sampling counter.

(C) Prior to the reset of the sample distributor, its contents are transferred to the sample hold register.

(D) Data in the sample hold register is compared with that in the address register. The address register counts the markers on the line.

(E) Upon coincidence (detected by the comparator), an extra memory unit is inserted in the histogram memory line.

(F) This memory unit is again extracted at the end of the line. The effect of this operation is that of augmenting by one space the particular section of the line. That is, all succeeding markers are shifted one step. The detail implementation of this operation is explained further in (I), central control.

(G) For each cycle of the delay line, the cumulator counts all spaces on the line. For review, the address register counts the markers, or *ones*, and the cumulator counts the spaces, or *zeros*. The number of *ones* and the number of *zeros* adds to the constant 1280.

(H) Connected to the cumulator are the quantile detector gates, which are simple coincidence gates, to detect coincidence between the present ordinates of the sample cumulative distribution. Upon coincidence of (G) and (H), the data in the address register constitutes the actual quantile values. The quantiles are, however, released only during an extra cycle. During this cycle, both the regular load operation and the marker realignment operation are inhibited.

(I) The central control unit includes:

(1) The automatic control of the sampling time to assume its compatibility with the incoming data rate and the available memory capacity.

(2) The automatic synchronization of the delay line.

(3) The preload and reload of markers.

(4) The regular load cycle.

(5) The quantile release.

The central control unit is now discussed in detail.

I(a). Automatic sampling control. The automatic sampling control consists of a reversible 8-bit binary control counter, an 8-bit frequency scaler, and an *and/or* gate network. For counting *up*, the control counter is augmented through an all-*zero* detector. This detector is connected to the sample distributor hold register. For counting *down*, the control counter is augmented through a full-scale or greater detector.

The control counter is allowed to reverse within a 5-bit span with no change in output frequency. The three most significant bits of the control counter are decoded. The decoded outputs are used to select the signal from one of the eight bits in the frequency divider. Any forward or reverse carry between the fifth and the sixth bit in the control counter constitutes a major reset command. To prevent oscillation between alternating *zero* and full-scale values of the distributor, a forward or reverse carry will not leave the remainder in an all-*zero* or all-*ones* condition respectively. Instead, the remainder in both cases is left in its half-scale condition. Fig. 50 shows this connection in block diagram form.

I(b). Serial memory control. In control of the histogram serial memory, two distinct events and one condition are distinguished: end of the line event; end of the sampling interval event; and out-of-sync condition, respectively.

In regard to the control logic, three areas are distinguished: automatic synchronization and event detection; preload or realignment of markers; control of the regular load operation.

The automatic synchronization and event detection circuitry is further divided into the following:

(1) Detection and correction of the condition of synchronism. An incorrect relationship between markers and spaces on the line is detected and the realignment circuitry activated.

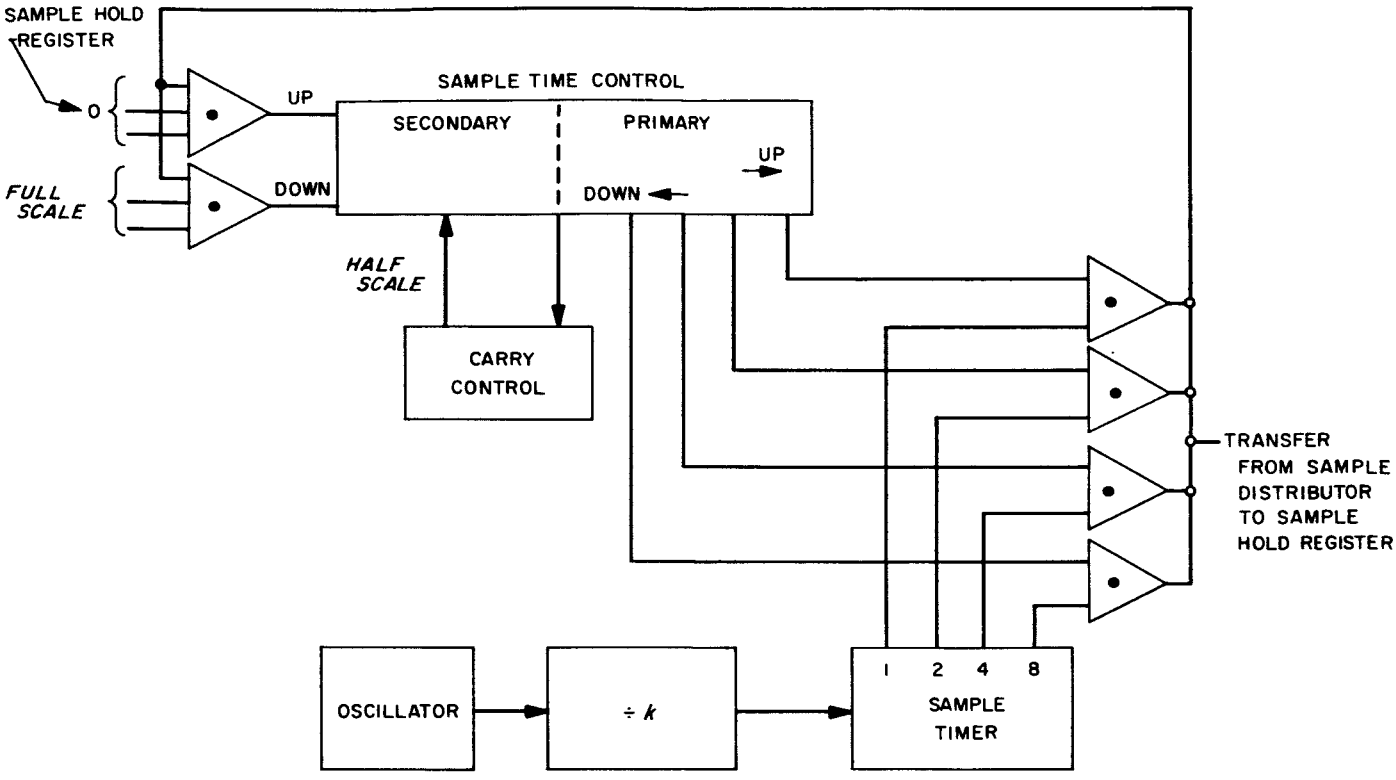


Fig. 50. Automatic sampling time control

(2) Detection of the end-of-line event. This signal is required in the regular load operation.

(3) Detection of the end of the sampling period. At this time, the quantiles can be released and the realignment of the markers occurs.

The preload or realignment of the markers' control logic controls the input to the serial memory. This memory shall thereby be made to recycle its own data, to enter *ones* continuously, or to enter *zeros* continuously.

The control of the regular load operation also controls the entry to the serial memory. During the load operation an extra one-unit-memory is added to or subtracted from the delay line.

Except for interconnections between the three control sections, three control terms external to the control unit are used: the *sample time* signal; the *address register full-scale* signal; the *cumulator full-scale* signal. In the following detail description of the control functions and their implementation, reference will be made to those major events that must occur, or to those conditions that must be satisfied, in order for a control bit to set or reset. Furthermore, the major functions of the control bit in question will be listed. For the actual connection between decision and memory elements reference is made to the logic diagram shown in Fig. 51.

I(c). Automatic synchronization, end-of-cycle, and end-of-sampling period detection. Control bits C1 through C5 control the synchronization and event detection for the proper operation of the serial memory. For every cycle of the memory line, one of four conditions is detected and registered:

C1: At the instant the address register reaches *full scale*, the cumulator has reached and remains at *full scale*.

C2: At the instant the address register reaches *full scale*, the cumulator is in a state other than *full scale*.

C3: At the instant the cumulator reaches *full scale*, the address register has reached and remained at *full scale*.

C4: At the instant the cumulator reaches *full scale*, the address register is in a state other than *full scale*.

A detailed discussion of C1–C4 follows; C5 will be introduced after discussion of C1.

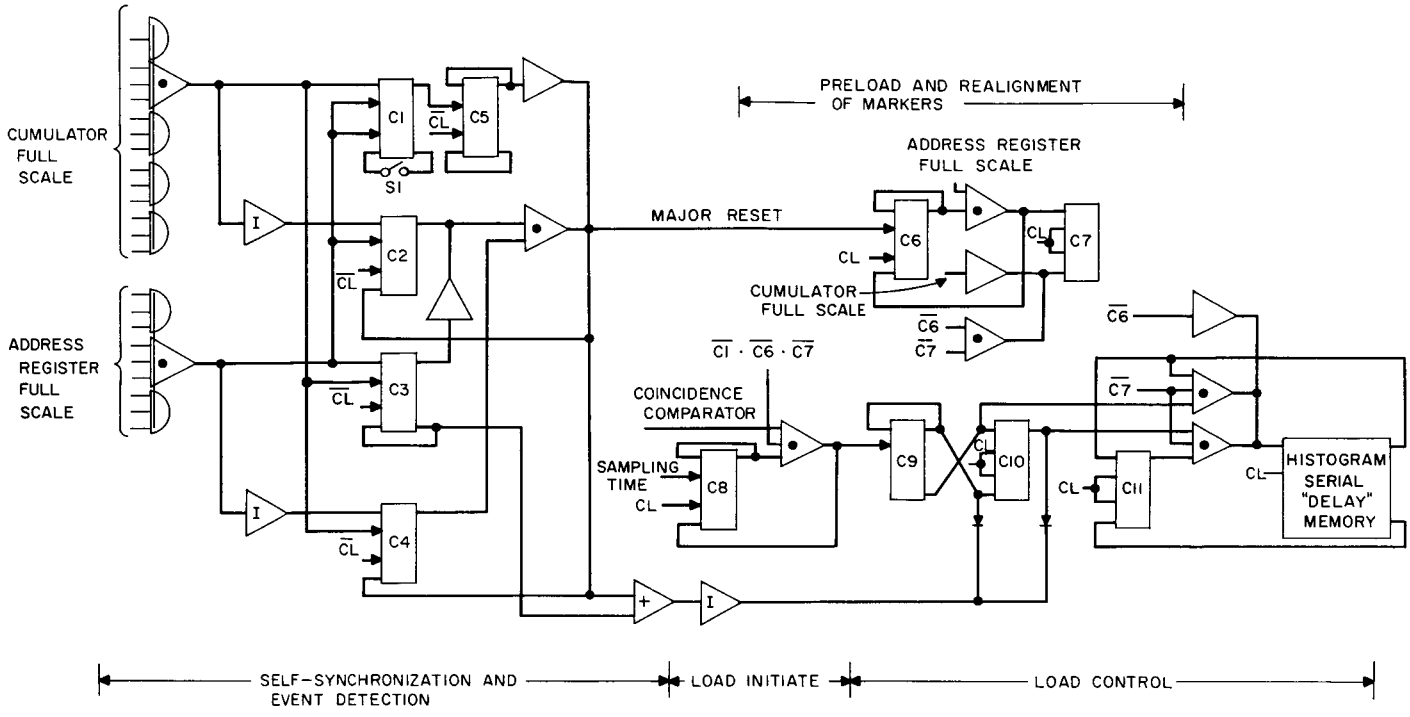


Fig. 51. Histogram serial memory control

C1 set indicates the completion of a sampling period; the quantiles can be released. C1 is again reset at the end of the readout cycle, at which time the address register again reaches *full scale*. (Realignment of the markers does not, however, take place during the readout cycle, because the address register is in fact identical to the quantile register during this readout cycle. The address register is time-shared in the subsequent realignment cycle, where it is utilized to tally the markers.) With S1 of Fig. 51 open, the completed histogram will recycle indefinitely for continuous readout of quantiles and for continuous display of the histogram. In closing S1, C1 will reset upon the next *address register full-scale* signal. Thereupon, the process of realignment and formation of the next histogram will begin. As C1 resets, C5 sets and resets again on the next half-clock period. This set and immediate reset action provides a signal which will activate the realignment circuitry and also provide an end-of-cycle signal.

C3 set indicates the end of the recycle period for the memory line. This C3 resets again on the next half-clock cycle. The C3 signal is used to reset or synchronize the address register, the cumulator (if not already reset through recycling), and the regular load control circuitry (C9 and C10 in Fig. 51). Reset of C3 at the next half-clock cycle will allow C9 and C10 to reset and again be operable at the next regular clock cycle. The condition that C2 is being set and not reset by C3 prior to the setting of C4, or the condition that, if C4 is being set and not reset by C1 prior to C2 setting, indicates a misalignment between the markers and spaces on the line. In other words, if ever C2 and C4 are both set simultaneously, this condition will reset C2 and C4 on the next half-clock cycle. The resulting signal constitutes a major reset and realignment signal of the same category as the C5 (end-of-sampling period) signal. The major reset signal also constitutes an end-of-line signal. It is interesting to note that for the case when the number of markers on the line amounts to a multiple of the capacity of the address register, this condition could temporarily appear as a line in sync. However, the misalignment would be detected soon thereafter during the regular load operation.

I(d). Preload and realignment of markers. C6 and C7 control the loading of *ones* and *zeros*, respectively. C1 is set by a major reset signal and it is reset by the *address register full-scale* signal. C6 controls the input to the memory line so as to enter *ones*. It also changes the input to the address register from the *ones* output of the memory line to the system clock. The address register reaches *full scale* when C6 is set; this causes C6 to reset and C7 to set. C7 controls the entry of *zeros* to the memory line and also changes the input to the cumulator from the *zeros* output of the memory line to the system

clock. If either C6 or C7 is set, the regular load operation is inhibited. If both C6 and C7 should inadvertently be set simultaneously, C7 is immediately reset.

I(e). Regular load operation. First consider the output from the sampling counter. This output is the transfer command which causes data from the distributor to be transferred to the hold register. Upon the very next coincidence between this hold register and the address register, the space between the marker that caused the coincidence and the next marker shall be lengthened by one unit. Only one coincidence per sampling time is being utilized (even though many more are likely to occur), since the utilization of coincidences is controlled by C8, which is set by the sampling time signal and reset by the first coincidence signal occurring thereafter. This sampling time signal is also used to set C9, which will inhibit, for one time unit, the entering of the output of the memory line to its input. Instead, a *zero* is entered. The data that normally would have been entered is stored in C11. Upon the next clock pulse, the data contained in C11 is entered into the line, and thereafter the memory line recycles through C11. At the end of memory cycle, both C9 and C10 are reset, which thereby again excludes C11 as a path for the recycling. This reset of C9 and C10 also allows simple recycling of the output to be directly connected to the input. This completes the discussion of the detailed logical design of the central control unit.

f. Outputs for advanced engineering quantile system. In addition to those features which are necessary for a flight version, the advanced engineering version needs extra output features, such as display. The type of display best suited for any one demonstration depends on the data rate and thereby the sampling rate also. The devices auxiliary to the quantiler are to do the following: print out all the histogram as well as the quantiles; analog display of the histogram as well as of the sample cumulative distribution on *X-Y* recorder and on an oscilloscope. The operation of the various auxiliary units will now be described.

Either of two functions can readily be displayed: the sample histogram, and the sample cumulative distribution. The technique of allowing the histogram memory to be represented by space between markers on a recycling delay line allows for the application of very simple cathode ray tube (CRT) display devices; these possibilities will now be discussed.

The cumulator is equipped with a display register and a digital-to-analog (D/A) network. Also, the regular quantiler address register is equipped with a D/A network. Upon completion of a histogram, one memory cycle is set aside for serial readout of the quantiles and for display of the histogram. For constant display, more than one cycle of the memory line will be required. In fact, the histogram can be displayed until erased through push button control (S1, Fig. 51). The same push button control will initiate the forming of a new histogram. The cumulative distribution function can be displayed continuously while the histogram is being formed, or it can be displayed in the same manner as the density function, as was described previously. With an added control bit, it is also possible to multiplex the display of the density function and the cumulative function.

The detail implementation of the display functions is depicted as follows: the transfer from the cumulator to the display register occurs on a marker. For display of the density function, the cumulator is also reset on a marker. For display of the cumulative function, the cumulator is not reset (except at *full scale* when it recycles through *zero*). If the display register D/A is applied to the vertical deflection, while the address register D/A is applied to the horizontal deflection, a display as shown in Fig. 52 will result. Fig. 53 is the block diagram of the functional units involved and their interconnection for this CRT display.

g. Conclusion. The quantile system described in this article requires a minimum of equipment, and would be

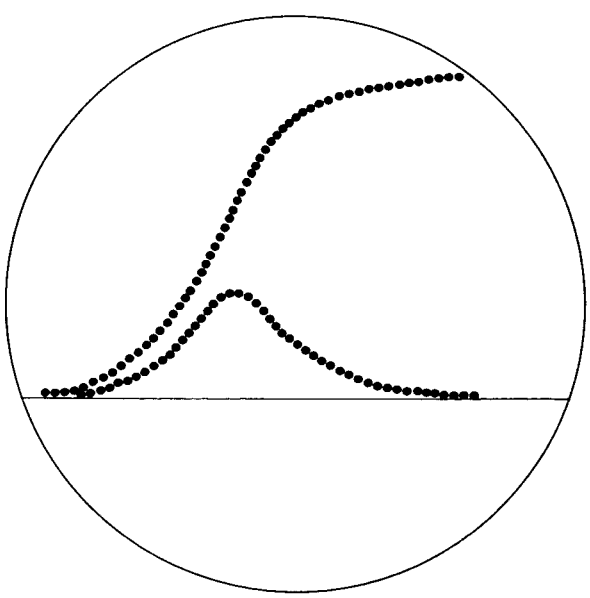


Fig. 52. Simultaneous density distribution display

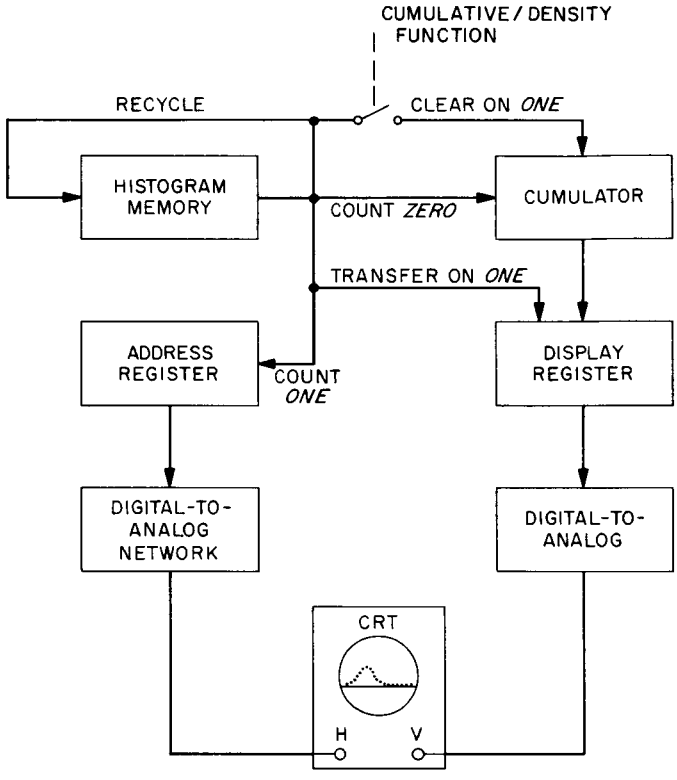


Fig. 53. CRT display block diagram

quite flyable on deep space missions. The advanced engineering quantiler being built is to demonstrate the feasibility of quantiles for data compression, and is one step removed from a flight model.

3. A Random Pulse Generator for Use As a Data and Noise Source

a. Summary. This article describes the design and theory of a random pulse generator for use both as a data source in advanced engineering projects involving compression of data for space telemetry, and as a source of noise for demonstrating coding schemes. As a data source, it will be used to demonstrate the quantile system of data compression (section 2 of this article). As a noise source, it will be used to generate a burst-error channel for demonstrating the punctured cyclic coding–decoding scheme (section 1 of this article).

The device itself is a deterministic machine, a maximal-length shift register generator (Refs. 38, and 39, p. 147) of long length. Events to be counted are determined by various functions of the output. The generator will be built using the new line of circuit modules (Ref. 40) developed in the Communications System Research Section.

b. Description. A length 36 maximal-length shift register generator is constructed, corresponding to the primitive polynomial of degree 36:

$$p(x) = x^{36} + x^{11} + 1,$$

whose degree is as high as is known for trinomials. However, for later work, one of the polynomials

$$p(x) = x^{127} + x + 1$$

(Ref. 41, p. 47, Corollary) or $x^{1023} + x^7 + 1$, if this last polynomial can be shown primitive, will be used, since the longer lengths are needed for the type of randomness required. These later versions would use a delay line, but this length 35 version will use a flip-flop shift register. At 1 Mc the length 36 will not repeat its starting length 36 window for 38 hr. Fig. 54 is a functional block diagram of the random pulse generator, and Fig. 55 shows the detailed logical design.

The pseudorandom events which are to denote pulses are available in four (nondisjoint) options:

Case I. A given length l, $1 \leq l \leq 7$, is selected on a 3-bit presettable binary counter. Also, a sequence of 0's and 1's of length l is chosen. A pulse is defined whenever the chosen window of length l occurs. After occurrence of the special sequence, the search begins again with no memory. Thus, if 11 is the special sequence, then the input 011100 records a pulse after the second 1, but not after the third 1.

Case II. A given number l, $1 \leq l \leq 7$, of cumulated 1's constitutes a pulse. After a pulse, the counter is reset. Thus, if three 1's are sought, the input sequence 00111*01000101*10 results in pulses at the starred positions.

Case III. A length l, $1 \leq l \leq 7$, is chosen, and consecutive disjoint blocks of length l are considered. A word of length l is chosen, which is allowed to include *don't care* positions. Pulses are defined whenever the given window occurs.

Case IV. The same as Case III, including *don't cares*, but instead of looking at nonoverlapping blocks, the block shifts by only one position each time. Thus, if the word 10

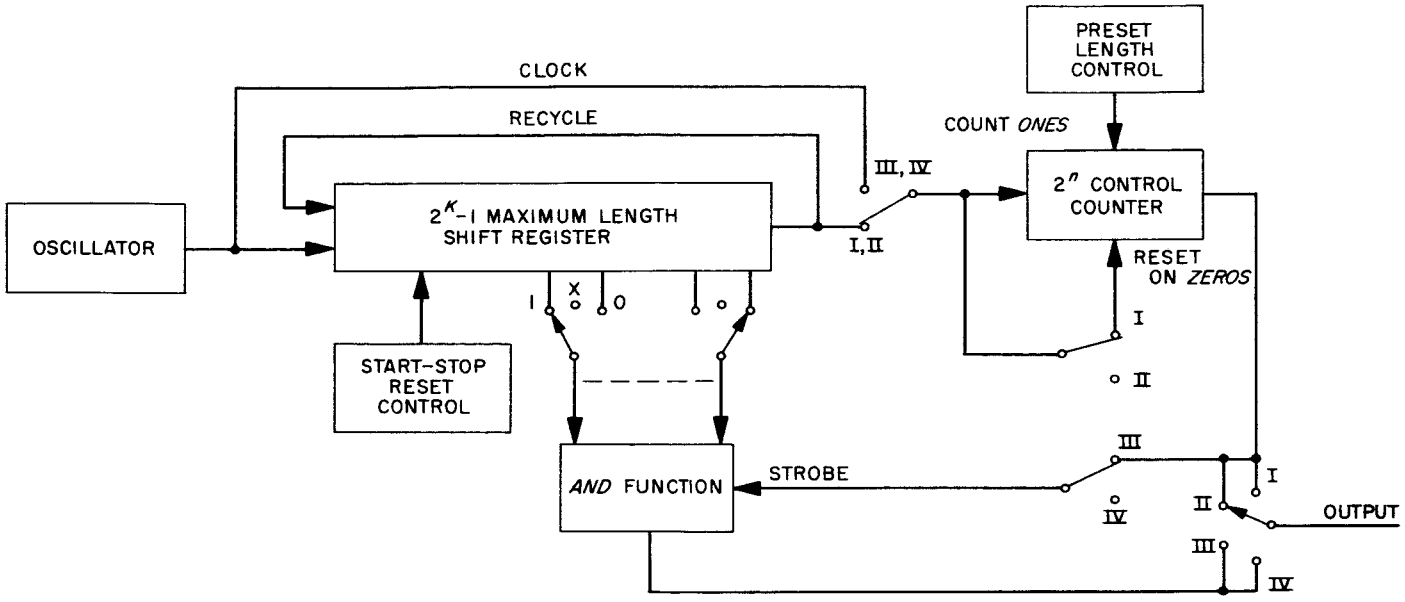


Fig. 54. Random pulse generator functional block diagram

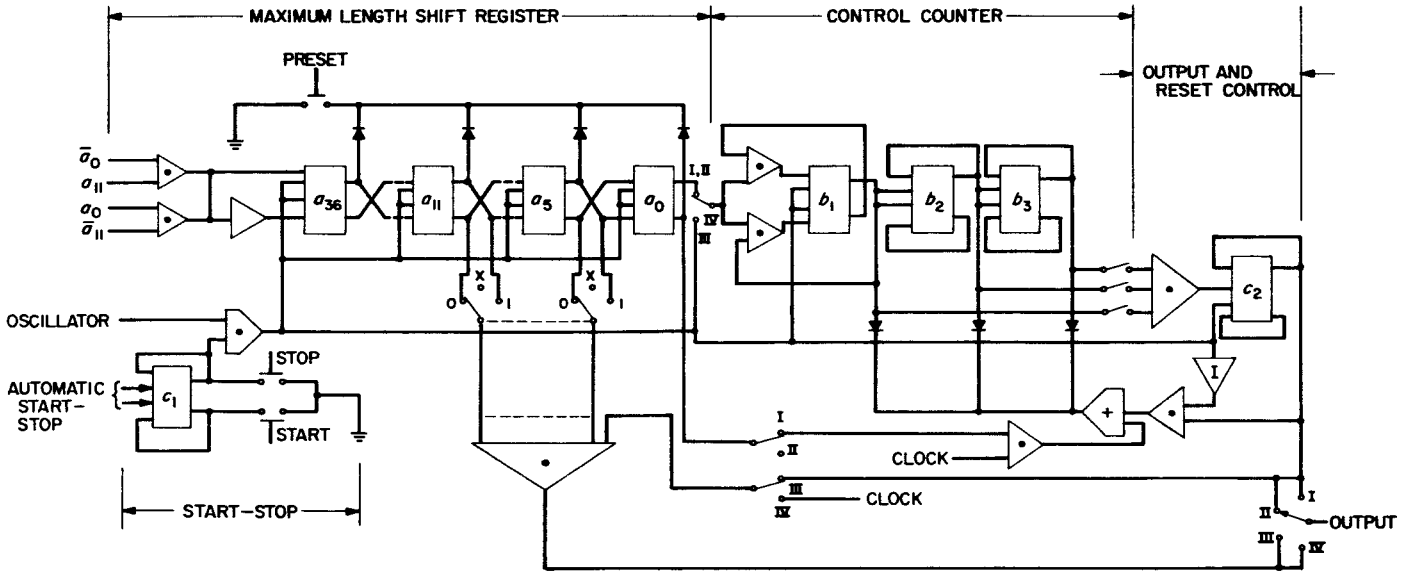


Fig. 55. Detailed design of random pulse generator

constitutes an event, then the sequence 0110*110* yields pulses at the starred positions.

c. Statistical properties of output. In order to make use of the flexibility provided by the above design, we will have to know the statistics of the pulses arriving according to the various schemes. Throughout this discussion, an input sequence of independent random variables which are 0 or 1 with probability ½ is assumed. This is a good assumption, since 2^{35} of the $2^{36} - 1$ terms in a single period of the output are 1's, and all windows of length 36 (other than the all-*zero* window) occur in a period. The statistics of the various output options will now be discussed together with the type of physical data source simulated.

In Case I this process is handled by the theory of recurrent events (Chap. XIII, especially section 7, of Ref. 42). In that terminology, we call a pulse a "run of length *l*." A closed-form expression for the distribution of waiting

times between pulses is best expressed in terms of the generating function

$$F(s) = \frac{(s/2)^l\,[1-(s/2)]}{1-s+(s/2)^{l+1}}.$$

The mean recurrence time is $\mu = 2^{l+1} - 2$, and the variance of the recurrence time is

$$\sigma^2 = \frac{2^{l+1} - 2l - 1}{2^{2(l+1)}} - 2.$$

In many applications of the random pulse generator, pulses are counted for a certain time and emptied into a counter. If this counting time n is long compared with l times the bit time, this theorem from Ref. 42 can be used: The number of occurrences in the first n bits, N_n, is approximately normally distributed with mean n/μ and variance $\sigma^2\,(n/\mu^3)$. This theorem applies for any persistent (sure to occur) recurrent (no memory once it occurs) event whose recurrence time has a finite variance. Thus, the theorem applies in the other cases below.

Using this theorem, we can obtain an approximately normal distribution of counts. By varying n and l, different means and variances are obtained. Actual particle sources also have statistics of this type, although the waiting time between events has, instead of a normal distribution of counts, a negative exponential distribution. But the distribution of counts in n bits, as n approaches infinity, converges to the normal distribution in the case of the negative exponential waiting time distribution, so that this artificial data source approximates a real one, at least for large n.

In Case II, techniques simpler than those in Case I are used to derive the distribution of waiting times for this recurrent event. The distribution of waiting times is the negative binomial

$$f_k = pr(\text{waiting time is } k) = \binom{k-1}{l-1} 2^{-k}.$$

The mean recurrence time is $\mu = l + 1$, the variance is $2l$. Again the normal approximation holds, but here the ratio of mean to standard deviation is more or less constant (in n). In Case I it was the mean-to-variance ratio of the normal that was approximately constant. Consequently Case II has a more concentrated distribution of counts than Case I.

In Case III we have nothing but a binomial distribution with p, the probability of success, equal to $1/2^{l^*}$, where $l - l^*$ is the number of *don't care* positions in the block of length l. Then $\mu = 2^{l^*} + 1$, $\sigma^2 = 2^{l^*} - 1$. This process will simulate many particle sources by the following reasoning. Particle counts in nature often have a Poisson distribution. And, for l^* large, with $2^{-l^*} \cdot n \sim \lambda$, the distribution of counts in n is approximately Poisson with parameter λ according to this distribution III, too.

Case IV embodies two cases: the first and last symbol in the block either agree or disagree. If they disagree, we have a recurrent event and the results are essentially the same as for Case I. But if the two symbols agree, then the event need not be recurrent, and new theory must be worked out.

For example, consider a pattern of four 1's. Once a run of 1's of length 4 has occurred, the probability of a pulse on the next shift is ½. The qualitative result is that the variance of the number of counts is higher here than in Case I.

To obtain more precise information is more difficult in this case than in the earlier cases, since the theory of recurrent events does not apply. Hence, the term "waiting time" is meaningless. All we can hope for at present is information of the distribution of pulses in n bits. While this problem has not yet been solved completely, we can compute at least the mean number E_n of pulses in n bits. Further details will be found in the next issue of *SPS*, Vol. IV.

To compute E_n, define a set of n random variables Y_i, $1 \leq i \leq n$, such that $Y_i = 1$ or 0 according as a pulse occurs at the ith bit. Then

$$\sum_{i=1}^{n} Y_i$$

is the random variable representing the number of pulses in n bits.

Let us say that the window of length l has $l - l^*$ *don't care* positions, and thus l^* "conditioned" positions. There is no possibility of recording a pulse unless $i \geq l$, due to the mechanization if not to the window chosen, so

$$Y_1 = Y_2 = \cdots = Y_{l-1} = 0.$$

$$\text{For } l \leq i \leq n,\ pr(Y_i = 1) = \frac{1}{2^{l^*}},$$

since there are l^* positions forced by the window. Thus

$$E(Y_i) = \frac{1}{2^{l^*}}, \qquad l \leq i \leq n.$$

Then

$$E_n = E\left(\sum_{i=1}^{n} Y_i\right) = \sum_{i=1}^{n} E(Y_i) = \sum_{i=l}^{n} \frac{1}{2^{l^*}} = \frac{n-l+1}{2^{l^*}},$$

the required expression. The variance of the number of pulses can be done similarly, and these calculations will appear in Vol. IV.

The statistical structure in Case IV has an interesting application in the synthesis of noisy channels. For, using a window of l 1's and calling pulses "errors," we see that burst-error patterns (Ref. 39, Chap. 10) are produced whenever a run of length greater than l appears. No way has been known previously of simulating burst errors in binary channels. This feature will be used to demonstrate the punctured cyclic coder–decoder.

d. Further refinements. In this section, we discuss other features present in the random pulse generator (Fig. 55). One feature that is useful is the ability to lock the counter. That is, we might need to have no pulses counted for some fixed r bit times after each pulse. This is a counter of the Type I in Ref. 42, p. 308. Or, we could demand a counter of Type II (Ref. 42, p. 308): if a particle arrives even during a locked period, the counter stays locked for r additional bits after this arrival.

The detailed design of the lockout procedures will now be described. A control bit C1 would set upon an output signal. Then, C1 would engage the time lock counter to cause lock for a presettable fixed number of bits. C1 would reset upon *full scale* of the time lock counter. During the time C1 is set the output would be inhibited for Type I. The Type II arrangement above would be mechanized as above except any intended output pulse occurring during the time that C1 is set would reset the time-lock counter again.

Another feature present is the following. In Ref. 43, the possibility was considered that particles arriving at the counter are from two distinct sources. Thus, we should like to be able to generate a mixture of two distributions. The case in which the mixture is bimodal (twin-peaked) is especially interesting. None of the four methods discussed gives distributions of bimodal type.

The way of obtaining bimodal distribution with this machine is to use lengths l_1 and l_2, respectively, where l_1 and l_2 can be unequal. If the correct window appears in the l_1 block, a particle of the first kind is said to arrive. If the correct window appears in the l_2 block, a particle of the second kind is said to arrive. A fundamental time unit is taken as $l_1 + l_2$, and one counting period consists of many $l_1 + l_2$ blocks.

The mechanization of this bimodality option will now be described. The length of the control counter would automatically vary for every other word synchronization pulse in the following manner. A control bit C2 would complement upon each word end. Thus controlled by C_1, the length would be l_1, whereas controlled by C2, the length would be l_2. Further variations in modality would be possible by a secondary control counter. This counter would vary the length of the primary control counter between $l_1, l_2, l_3, \cdots, l_n$.

In conclusion, the random pulse generator described here is a versatile source of distributions of both data for demonstrating data-compression systems, and of noise for demonstrating coding systems.

F. Digital Development

1. Mod III Auxiliaries Rack

a. Introduction. While the Mod III ranging equipment stored program controller (SPC) was still under construction, it was determined by experience with the Mod II SPC, that the complement of input/output equipment to be included with the Mod III would be insufficient for the full use of the equipment as a component of an operational system.

Early in 1963 a proposal was distributed, outlining the requirements for additional equipment. Subsequent meetings and discussions have resulted in the complement of equipment called the Mod III auxiliaries rack.

Construction of the auxiliaries rack was started in August 1963. Final testing had been completed by mid-January with installation at GTS by February 1.

The primary purpose of the auxiliaries rack is to provide the operating personnel with additional equipment for the display, in real time, of results and other pertinent information regarding the experiment in progress. The

secondary function of the equipment is to provide the experimenter with more versatile computer output equipment in order to display the results of the reduced experimental data gathered during the operations.

The auxiliaries rack consists of an octal display of 9 digits, a binary-coded decimal (BCD) display of 9 digits, 10 digital-to-analog converters (two 10-bit and eight 8-bit), an *X-Y* recorder, an 8-channel stripchart recorder, a 300-character/sec paper tape reader, a bidirectional paper tape spooler, and the necessary additional interface equipment for the proper operation of the above equipment with the Mod III (Fig. 56).

The displays are included to present, in a clearly readable form, selected words of data such as time, range, signal-to-noise ratio, range uncertainty, etc., during an operation, and orders or data within the controller during program debugging.

The digital-to-analog converters (DACs) are provided to convert the controller-generated digital words into

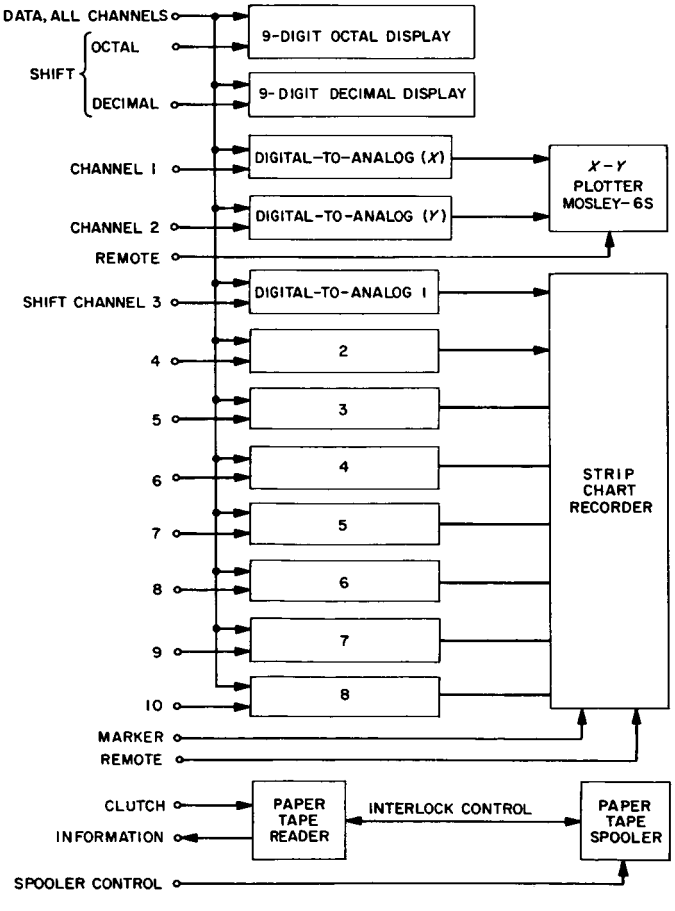


Fig. 56. Mod III auxiliaries rack block diagram

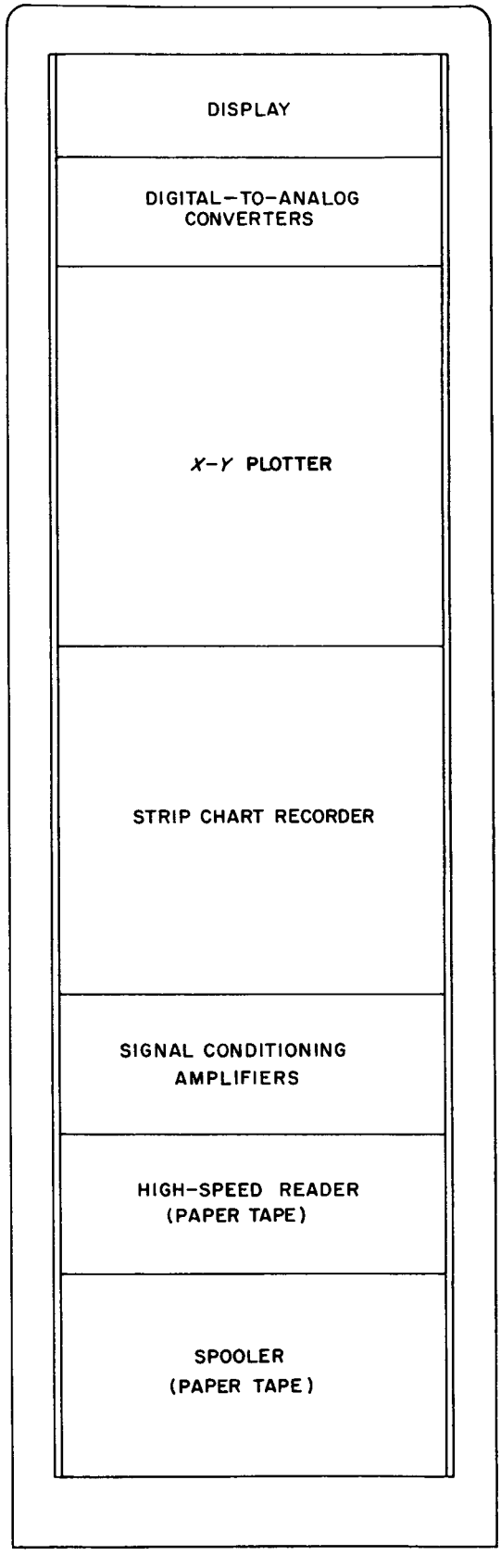


Fig. 57. Mod III auxiliaries rack

analog signals to drive the recorders. These DACs are constructed on a two's complement basis with the range of their outputs being zero to −10 v. A zero into the DACs will produce a −5-v output. Since the recorders used have bipolar inputs and zero offset this convention imposes no restriction on the system.

The paper tape reader was provided for flexibility in operations and as a second data entry station for *off*-line data reduction.

All of the above equipment is mounted in a Venus site standard rack (Fig. 57). The interconnections are made at the rear of the rack. The inputs and outputs of the auxiliaries rack are through an interface panel mounted on the floor of the rack.

In order to control the electrical noise in the auxiliaries rack, the mounting rails (both front and back) are tied together to form a solid signal ground. Although the power ground is also tied to this point by the construction of the units used, the power is returned on a separate buss for each unit.

All subsystems were built as self-contained units as a pattern for similar units which may be used independently.

b. Octal-decimal display. In line with the general philosophy of design, this unit was constructed to stand alone; it has its own power supplies and driving circuits. Fig. 58 is a block diagram of the display. Information from the SPC enters the display and is reshaped, then shifted on an appropriate shift command into either of the display registers where it is stored until replaced. Bits in the register drive relays which, in turn, decode each group of 3 (for octal) or 4 (for decimal) into 8- or 12-line outputs which activate the numerical indicator display lamps.

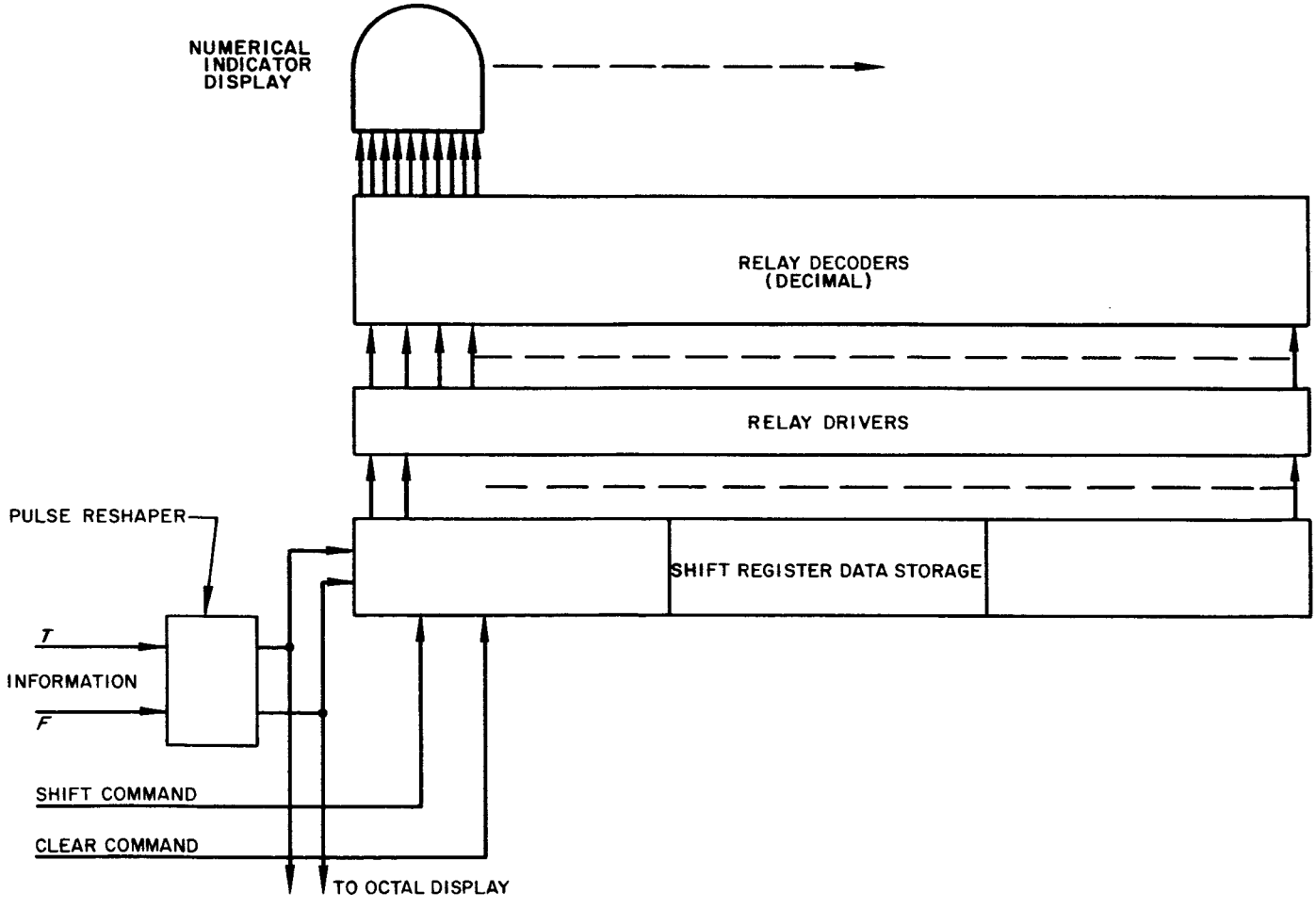


Fig. 58. Display block diagram

A push button is provided for each register to reset it to zero.

c. Digital-to-analog converter subsystem. This unit was also constructed to work by itself and as such contains all the necessary power supplies and driver circuits. Fig. 59 is a block diagram of the DAC unit. Information entering the unit from the SPC is reshaped and shifted into the appropriate register. The output of this register drives current switches which in turn drive the ladder networks.

The state of each flip-flop in the register is displayed on the front panel. A push button is provided for each flip-flop which will set it, thereby manually entering a number into the DAC. A push button is also provided for each register which will clear the register.

The indicators and push buttons for the 8-bit registers are switched between the registers as required.

d. Interface. The interface components were chosen to provide both isolation and conditioning of signals into, and out of, the auxiliaries rack.

All information signals are run through coaxial cables terminated at the receiving end.

All binary control signals originate in the stored program controller as relay contact closures which are repeated by buffered mercury relays in the auxiliaries rack. These in turn operate the circuits internal to the units being controlled.

The only piece of equipment needing an interface additional to that mentioned above was the tape spooler. It was necessary to provide an additional relay to switch the inputs when in remote operation. This addition allowed the manual operation to be maintained.

With the exception of the extra relay on the spooler all the interface relays are mounted on a panel at the

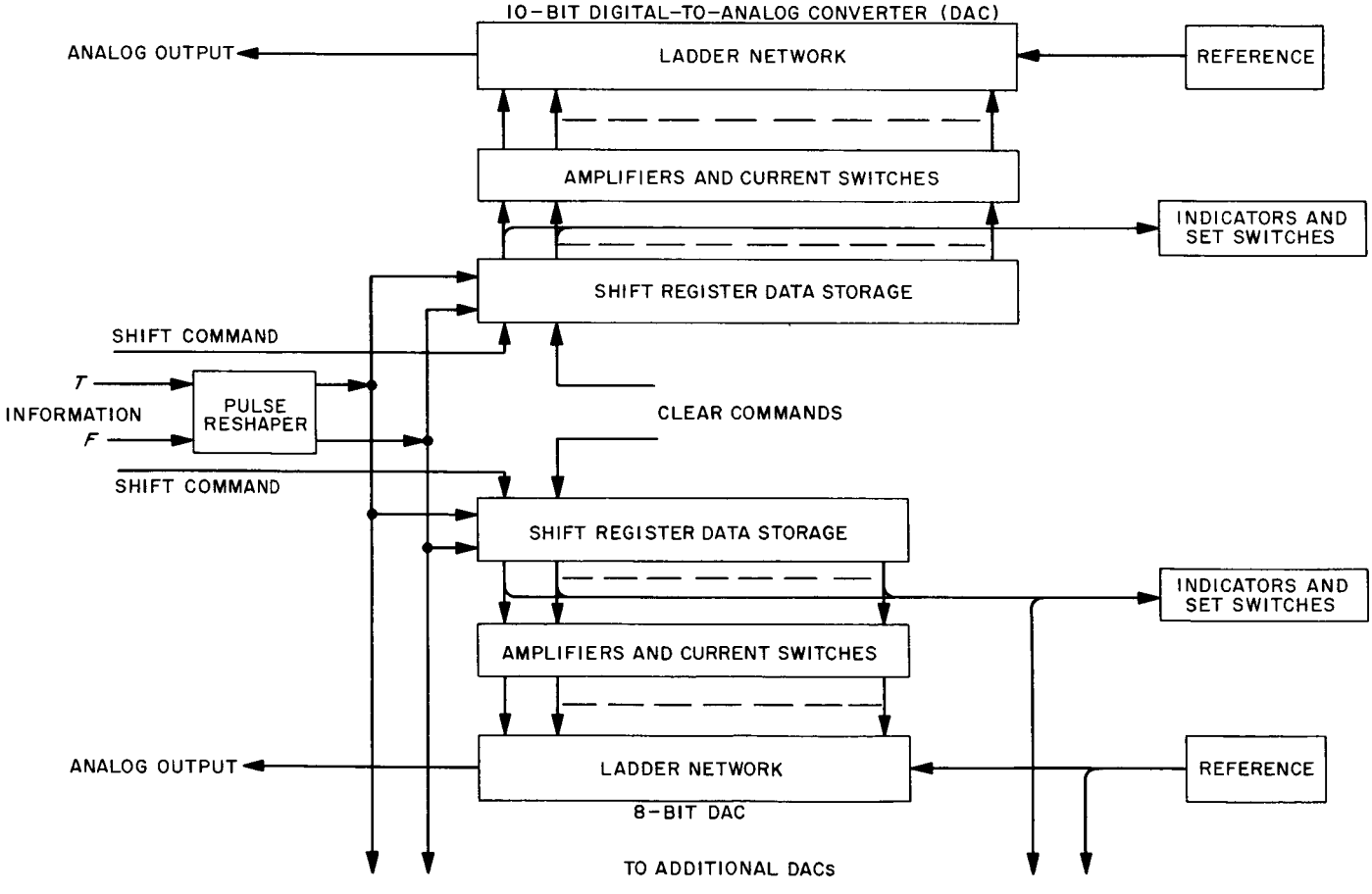


Fig. 59. DAC block diagram

rear of the auxilaries rack. This panel is easily accessible for changes and additions, as they become necessary.

2. Voltage Multiplexer for Stored Program Controller

a. Introduction. Many of the tasks to be performed by either the Mod II or III stored program controller (SPC) require the ability to sample an analog voltage, converting the measurement to a number which the arithmetic unit can process. For example, in transponder ranging operations, the SPC monitors the correlation output of the receiver as the ranging coders are shifted during the acquisition procedure. In RF acquisition experiments the SPC uses the output of a strong-signal discriminator to guide its operations during the acquisition of the down-link signal, and then applies digital filtering techniques to the ground receiver's static phase error output to assist in recognition of the transponder's acquisition of the up-link signal.

The device used to perform these tasks is an analog-to-digital converter (ADC), in this case a Voldicon unit made by Adage, Inc. It is capable of converting a voltage into a number consisting of ten binary digits and sign, performing the conversion in approximately 50 μsec. The SPC makes use of the ADC by triggering it once for each order the machine performs, doing this at such a time that if the next order asks for a number from the ADC, the number is immediately available. The ADC includes a sample-and-hold input amplifier so that each conversion is performed on a precisely timed sample of the input signal.

b. Need for multiplexing. An extension of this facility is to be used in lunar radar experiments where the SPC will have to read several instruments (three or more) in rapid succession, determine which readings are within the scale limits for the instruments, and feed the proper values into the control and data processing programs. The basic Voldicon unit has a single analog input which could be switched from one instrument to another by means of relays but this would be too slow for the lunar radar operation. The only acceptable solutions would be to use several ADC units (which would be very expensive) or to provide for electronic switching of channels, i.e., multiplexing selected voltages into the ADC input.

c. Voldicon multiplexer. The Voldicon is a self-contained unit, built in a conventional "card-cage," typical of most digital system construction, and it has space which can be used for mounting additional cards. Adage, Inc. makes a number of multiplexer cards, as well as the gating and control cards required to integrate the multiplexer into the ADC, so the Mod II SPC's ADC was returned to the factory to have a ten-channel multiplexer installed, along with the additional switching and controls required. This unit has been tested in the Mod II and will be installed in Mod III for use in future operations.

d. Multiplexer operation. The multiplexer consists of ten electronic switches that select the desired input lines and connect them to a common bus which is fed through another switch to the input of the sample and hold amplifier. The output of the amplifier is fed back to the switches in such a way that the switches are inside the loop and any minor offsets or drifts in the switches are compensated for by the high gain of the amplifier (Fig. 60). The sum of all selected input voltages charges the storage capacitor C each time a *sample* pulse is received. The *hold* command follows 20 μsec after the start of the *sample* pulse and causes the amplifier output to remain constant during the conversion process. On completion of conversion the *restore* command discharges the storage capacitor and stabilizes the amplifier until the next sample is required.

It is interesting to note that when a channel is not selected, its input resistor returns to ground through the input switch. When that channel is selected, the input is connected to a virtual ground, the summing junction of the amplifier, which is always held close to ground by the

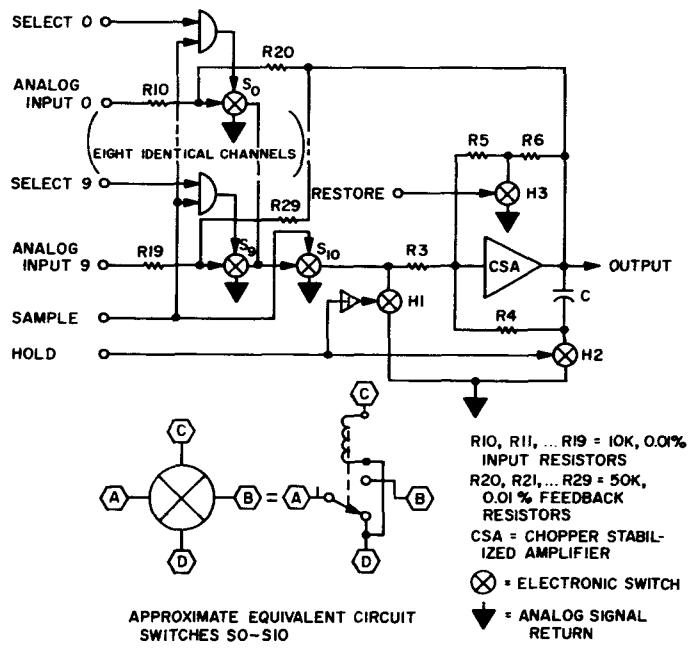


Fig. 60. *Sample* and *hold* with multiplexer

gain of the amplifier and the feedback system. At the beginning of a sampling pulse there is a transient at the summing junction as the amplifier "homes in" on the input signal, but the input source is isolated from this transient by the input resistor. The fact that the input impedance is constant, and that the storage capacitor is discharged after each sample, greatly reduces the possibility of crosstalk between channels.

e. Operation with SPC. SPC triggers the multiplexer-ADC unit once for each order processed. The trigger is timed so that the *sample* pulse is enveloped by the *data read-in* cycle of the SPC and conversion starts just after the end of *data read-in*. Fig. 61 shows the time relation of the various cycles.

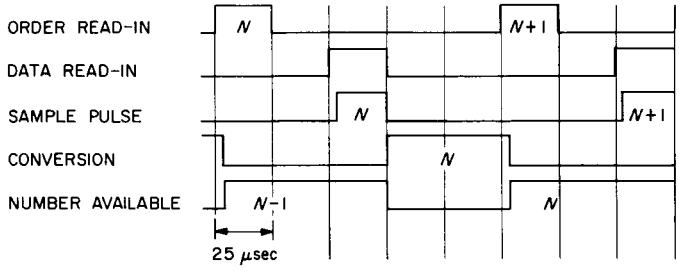


Fig. 61. SPC multiplexer timing

When order N is read in, the converter is just finishing sample $N - 1$, so that is the value which will be available if order N requests a number from ADC. During the *data read-in* cycle for order N a *sample* pulse initiates the conversion of sample N which, in turn, will be available for read-in during order $N + 1$.

The ten multiplexer channels are selected by SPC flip-flops whose addresses are 23040 to 23051, inclusive. If a channel is to be used for a number of readings, and several different orders are to address the ADC (20207), the best strategy would be to set the flip-flop beforehand, leaving that channel permanently selected for as long as desired, resetting the flip-flop at the end of the period where that channel is used. In this mode, note that the selected flip-flop turns *on* at the beginning of the *data read-in* cycle, so the next order can read the output of that channel. If, on the other hand, the program requires isolated readings from assorted channels, it would be better to pulse the flip-flop for each channel on the order immediately preceding the order which requests the number. That is, on order N pulse the flip-flop (which will be on for the duration of the *data read-in* cycle) will envelop the sample pulse, and on order $N + 1$ will read the number resulting from the conversion.

For example, if the program requires the difference between the voltage on Channel 0 (23040) and the voltage on Channel 6 (23046) this program could be used:

PSE, +23040 (Pulse flip-flop to select Channel 0).

CLA, +20207 (Clear and add numerical value of Channel 0).

PSE, +23046 (Pulse flip-flop to select Channel 6).

SUB, +20207 (Subtract numerical value of Channel 6).

One other address pertaining to the ADC system is 20211 which has the mnemonic symbol ABS (for absolute value). A signed number which is proportional to the input voltage is produced by 20207 (ADC), while 20211 (ABS) produces a number which is the positive absolute value of the number which appears at 20207. If the ADC system is being used for power measurements, the normal procedure would be to sum the squares of the voltage readings as a step in determining the rms value. In certain cases, particularly when the mean voltage is known to be zero, the sum of the absolute value of the voltage readings can be used as a representation of the power, so the addition of the ABS option to the ADC system can simplify and speed up the operation in such cases.

f. Performance. To check the performance of the multiplexer-ADC unit, it was installed temporarily in the Mod II SPC with all the analog inputs tied together so they could be fed from a common signal source. No attempt was made to refine the signal grounding system nor was shielded wire used; the intent was to get a pessimistic rather than an overly optimistic evaluation of the system. When a signal other than zero was used the signal generator was adjusted so that its peak excursions did not quite saturate the ADC, so the amplitude of the test signal was ±1 v, or 2 v peak-to-peak.

Fig. 62(a) shows a histogram of the occurrences of various readings for each of the channels when the common input to all channels was connected to ground. A period (.) represents a 0, the first (x) represents a 1, and each additional (x) represents twice as many events as the previous one. Thus a bar of 10 x's represents approximately 1024, so that the plot is essentially a Base-2 logarithmic scale.

Fig. 62(b) shows the results obtained by sampling a given channel and immediately afterward subtracting a reading of Channel 0. Since one would normally expect a spread of ± 1 on a given reading, the fact that these distributions cover a range of ± 2 is reasonable. Incidentally, one unit in a reading is almost 1 mv.

Fig. 63 shows the results of reading two channels in rapid succession and differencing their values, with a sine wave input. Since the voltage can change between two readings one would expect a double-peaked curve, particularly at the higher frequency. Also, since a sine wave has a high amplitude for a greater percentage of

(a) DISTRIBUTION OF CHANNEL READINGS FOR ZERO VOLTAGE INPUT

	CHANNEL 0	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4	CHANNEL 5	CHANNEL 6	CHANNEL 7	CHANNEL 8	CHANNEL 9
+5	•	•	•	•	•	•	•	•	•	•
+4	•	•	•	•	•	•	•	•	•	•
+3	•	•	•	•	•	•	•	•	•	•
+2	•	•	•	xxx	•	•	•	•	•	•
+1	•	xx	xxx	x	•	xxxx	xxxxx	xxxx	x	xxxxxx
0	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx
-1	•	•	•	•	xxx	•	•	•	xx	x
-2	xx	xx	•	•	xxxxxxxx	x	•	•	xxxxx	xxx
-3	•	•	•	•	xxxxx	•	•	•	•	•
-4	•	•	•	•	•	•	•	•	•	•
-5	•	•	•	•	•	•	•	•	•	•

(b) DISTRIBUTION OF DIFFERENCES BETWEEN CHANNEL READINGS FOR ZERO VOLTAGE INPUT; 4096 SAMPLES AT 250 SAMPLES/sec (BASE-2 LOG PLOT)

	CHANNEL 0-0	CHANNEL 1-0	CHANNEL 2-0	CHANNEL 3-0	CHANNEL 4-0	CHANNEL 5-0	CHANNEL 6-0	CHANNEL 7-0	CHANNEL 8-0	CHANNEL 9-0
+5	•	•	•	•	•	•	•	•	•	•
+4	•	•	•	•	•	•	•	•	•	•
+3	•	•	•	•	•	•	•	•	•	•
+2	xxxxxxxxx	xxxxxxxxx	xxxxxxxx	xxxxxx	xxxxxxx	xxxxxx	xxxx	xxxxx	xxxxxxx	•
+1	•	xxxx	xxx	xx	xx	xx	x	xx	xx	•
0	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx
-1	xx	xxx	xx	xxx	xxx	xxxxx	xxxxxx	xxxxx	xxx	xxxxxxxxx
-2	xxxxx	xxxxxx	xxxxx	xxxxx	xxx	xxx	xxxx	xxxx	xxxx	xxxxx
-3	•	•	•	•	•	•	•	•	•	•
-4	•	•	•	•	•	•	•	•	•	•
-5	•	•	•	•	•	•	•	•	•	•

Fig. 62. Channel offsets

(a) DISTRIBUTION OF DIFFERENCES BETWEEN CHANNEL READINGS FOR 2-v PEAK-TO-PEAK, 1-cps SINE WAVE; 4096 SAMPLES AT 250 SAMPLE/sec (BASE-2 LOG PLOT)

	CHANNEL 0-0	CHANNEL 1-0	CHANNEL 2-0	CHANNEL 3-0	CHANNEL 4-0	CHANNEL 5-0	CHANNEL 6-0	CHANNEL 7-0	CHANNEL 8-0	CHANNEL 9-0
+5	•	•	•	•	x	•	•	•	•	•
+4	xxxx	xxxxx	xxxx	xxxx	xxxxx	xxxx	xxxxx	xxxx	xxxx	x
+3	xxxxxx	xxxxxxx	xxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxxx	xxxxxxx	xxxxxxxx	xxxxxxx
+2	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx
+1	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx
0	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx
-1	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx
-2	xxxxxx	xxxxxx	xxxxxx	xxxxxx	xxxx	xxxxx	xxxxx	xxxxx	xxxxx	xxxxxxx
-3	•	•	•	•	•	x	•	•	•	xx
-4	•	•	•	•	•	•	•	•	•	•
-5	•	•	•	•	•	•	•	•	•	•

(b) DISTRIBUTION OF DIFFERENCES BETWEEN CHANNEL READINGS FOR 2-v PEAK-TO-PEAK, 0.1-cps SINE WAVE; 4096 SAMPLES AT 250 SAMPLES/sec (BASE-2 LOG PLOT)

	CHANNEL 0-0	CHANNEL 0-1	CHANNEL 0-2	CHANNEL 0-3	CHANNEL 0-4	CHANNEL 0-5	CHANNEL 0-6	CHANNEL 0-7	CHANNEL 0-8	CHANNEL 0-9
+5	•	•	•	•	•	•	•	•	•	•
+4	•	•	•	•	•	•	•	•	•	•
+3	xx	xx	x	xxx	xxxx	xx	xxx	xxx	xxx	•
+2	xxxxxxxxx	xxxxxxxxx	xxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx	xxxxxxx
+1	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx
0	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx	xxxxxxxxxx
-1	xxxxx	xxxx	xxxxx	xxx	x	xxx	•	xxx	xx	xxxxxx
-2	•	•	x	x	•	x	x	x	•	x
-3	•	•	•	•	•	•	•	•	•	•
-4	•	•	•	•	•	•	•	•	•	•
-5	•	•	•	•	•	•	•	•	•	•

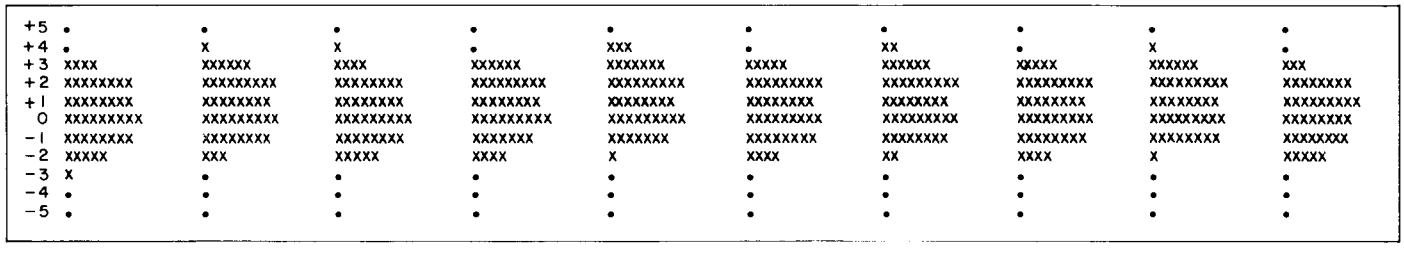
Fig. 63. Gain differences, sine wave

its cycle, if there are differences in the gains of two channels, one would expect a wider spread than that observed with a triangular wave input.

Fig. 64(a) shows the distribution obtained when the input is a triangular wave. It appears that there is an over-all bias in the distributions, so the test was run again, this time reading Channel 0 first and then the variable channel. The curves in Fig. 64(b) appear to be biased in the opposite direction by a slight amount, indicating that the first reading after a period of inactivity is likely to be slightly less than one taken a short time later. However, since the shift is less than ½ bit, it is no cause for concern.

For Fig. 65, a square-wave input was used. The readings at the outer ends of the distributions represent differences of five or more, and represent the instances when a pair of readings straddled a transition of the square wave. The remaining portions of the curves show much less spreading than was noted in the sine- and triangle-wave cases, since after the end effects are eliminated, the rest of the readings are being taken on essentially stationary voltages. This set of curves shows that

(a) DISTRIBUTION OF DIFFERENCES BETWEEN CHANNELS FOR 2-v PEAK-TO-PEAK, 1-cps TRIANGLE WAVE; 1000 SAMPLES AT 250 SAMPLES/sec (BASE-2 LOG PLOT)



(b) DISTRIBUTION OF DIFFERENCES BETWEEN CHANNELS (VARIABLE CHANNEL SECOND) FOR 2-v PEAK-TO-PEAK, 1-cps TRIANGLE WAVE; 1000 SAMPLES AT 250 SAMPLES/sec (BASE-2 LOG PLOT)

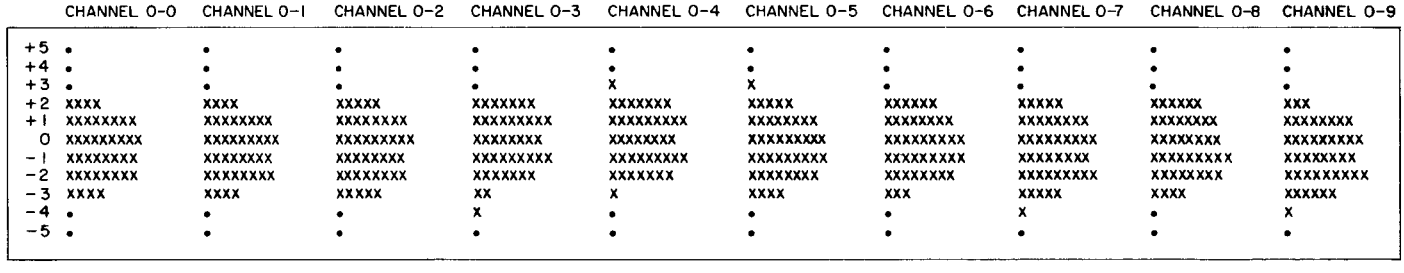


Fig. 64. Gain differences, triangle wave

DISTRIBUTION OF DIFFERENCES BETWEEN CHANNELS FOR 2-v PEAK-TO-PEAK, 1-cps SQUARE WAVE; 4096 SAMPLES AT 250 SAMPLES/sec (BASE-2 LOG PLOT)

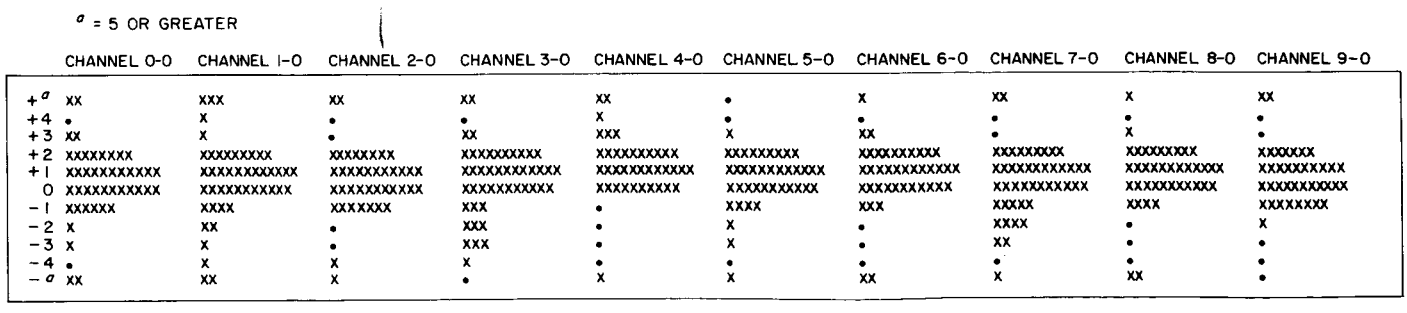


Fig. 65. Gain differences, square wave

the channels have a net offset of ±1 count and a gain variation of ±1 count over their full-scale range.

Fig. 66 shows the result of combining all the differences in reading pairs without regard for channel. All channels were used uniformly, and since the input was a triangle we expect a broad distribution. Here again, though, the bulk of the readings are within ±2 units.

These results lead to the conclusion that readings taken with the multiplexer-ADC-SPC system should be correct to within ±0.1% which is probably better than the analog data source with which it will be used. If the analog sources are calibrated by using the SPC to read their voltages, then the multiplexer channel will be included in the instrument calibration.

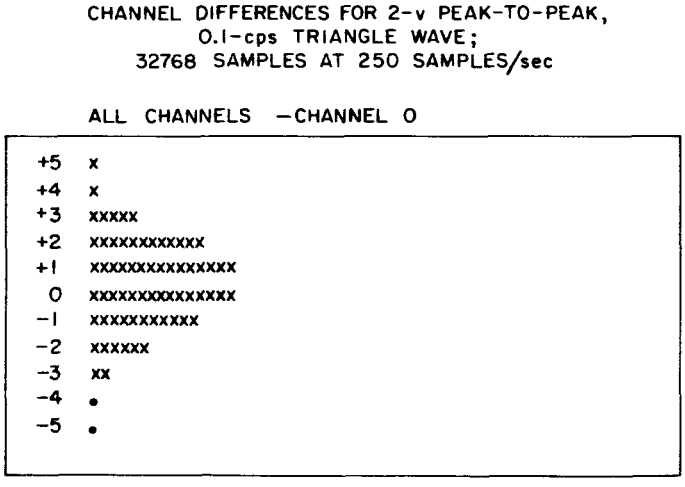


Fig. 66. Composite gain differences

3. Evaluation of Digital Circuit Modules Procured under JPL-Owned Design

a. Introduction. Described here are tests performed on modules supplied by the Control Logic Corp. for the digital modules procurement program, last described in Ref. 44. These are circuits owned by JPL, and being fabricated also by two other manufacturers, Walkirt and Applied Development. The modules are plotted on cards and ultimately will use a connector developed by Applied Development under contract to JPL. The tests described here are performed on the memory element (or flip-flop) and on the decision element (or gate). The result of the tests is that all JPL specifications (GM2-15053-DSN-B) were met or exceeded.

b. Type of tests. Without additional information, the label that a set of digital circuits (i.e., a *nand* gate and associated RS[1] flip-flop) is a 2-, 3-, or 5-Mc line is insufficient. The additional information referred to may be, for example, the *combination rules*; that is, how many levels of gating between flip-flops are considered in a synchronous system? It may also be *loading rules*; that is, how many elements of one or another kind is the output of an element expected to drive, with the combination rules still being valid?

Still more information is necessary. Under what supply voltage conditions are the above rules true? And under what environmental conditions, particularly the ambient temperature, are the *combination* and *loading rules* true? Further pieces of information necessary for an evaluation of a set of digital circuits are: Under what noise conditions are the rules true? And under which component deterioration conditions are the rules true?

Conversely, a set of digital circuits may be evaluated on the basis of the exact waveforms: the minimum input waveform requirement for triggering of the flip-flop, for example, and the output waveform resulting from a certain input waveform under various loads, supply voltages and environmental conditions to mention but two important criteria. For the *nand* gate, the *turn-on delay*, the *turn-on switching time*, the *turn-off delay* and the *turn-off switching time* are the important parameters. The delay time is the time between the beginning of the input and output transitions. The switching time is the time between the beginning and end of the transition measured at 10% from the initial and final level.

For the flip-flop, the parameters of interest are the minimum time required for the enable level to be true prior to the beginning of the clock transition, the absolute swing of the clock transition, as well as its switching time for the flip-flop to set or reset. The switching delay, that is, the time between the beginning of the clock transition and the beginning of the output transitions, are other values of interest as well as the time difference between the beginning of the set output transition and the beginning of the reset output transition. Of equal interest is switching time for set and reset outputs.

Regarding delay and switching times, more practical definitions may be the propagation time for each element. The average propagation time for the *nand* gate can be measured by connecting a large odd number of elements in a series and dividing the time delay between the input to the first and output of the last by the number of elements. (In fact, if the output is connected back to the

[1]RS: Reset-set.

input the loop will oscillate. The period of the frequency of the oscillation is also a measure of the propagation time.)

c. Description of tests of the flip-flop. Two methods of describing or evaluating a set of digital circuits have been outlined: that of specifying the *combination* and *loading rules* in relation to the operation required under all environmental conditions, and that of describing the input–output waveforms under all conditions. Because of the large number of variables and values for each variable, the total number of combinations that must be covered for a complete evaluation is large (for either of the two methods). In addition, a complete evaluation cannot be based on a single element but must include the variation in performance between a large number of elements.

In view of what has been stated, the actual testing program that has been carried out and which will be reported on here, is a part of the full set of tests that could be performed. Thus, after a number of preliminary experiments had been performed in order to gain a first indication of the general capability of the circuits, a special test jig was designed which included a typical but rather stringent systems application. The preliminary experiments that led to the design of this test jig will now be described in detail.

To determine the average propagation time for the flip-flop, each of a large number of flip-flops is connected so as to complement on a transition applied to the set and reset triggers in parallel. The output of one flip-flop is used as the clock transition for the next. This connection is known as the binary ripple counter. Under ideal laboratory conditions, the average ripple propagation delay between 10 flip-flops so connected was registered to be on the order of 25 nsec for each stage.

In an experiment designed as a qualitative measurement, the flip-flop was connected, as shown in Fig. 67, with various types of loads. Flip-flop B is the one to which the various loads were attached. The shift from A to B is included in order to make B operative with its outputs unloaded. Flip-flop C is the malfunction detector. As in a true system configuration, the clock in these experiments was derived from a decision element. The clock used was of a symmetrical waveform. The loads were also symmetrical.

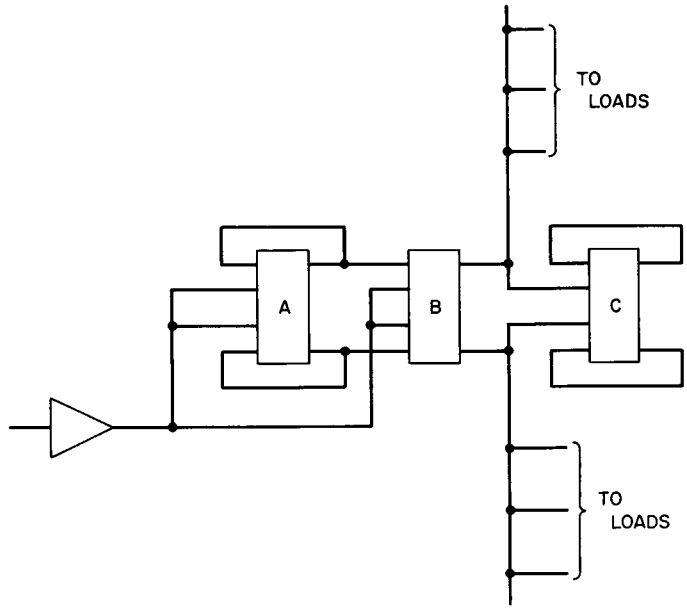


Fig. 67. Flip-flop load and speed test

First, the maximum operating frequency was measured at specified loads. Second, the maximum drive capability at specified operating frequency was recorded. The specified loads were:

Four decision elements, or

Eight F-F enable loads, or

Two F-F trigger loads.

Included in the number of decision element loads is the trigger input to the secondary flip-flop regarded as two decision elements. The same load is also included in the number of F-F enable loads and regarded as four enable loads. And the specified frequency was 3 Mc square wave.

Table 8 is the result of the experiments to determine the maximum operating frequency at specified maximum load. As is shown, the circuits operated at twice the specified frequency, or higher.

Table 8. Results from experiments to determine the maximum operating frequency for the memory element at specified loads

Type of load	Decision element	Enable	Trigger
Maximum loads specified	4	8	2
Maximum specified frequency, Mc	3	3	3
Measured operating maximum frequency, Mc	7.5	7	6

The frequency noted was that prior to any malfunction of either the driving flip-flop or any of the flip-flops that were driven. In this connection, it may be mentioned that the trigger action of the flip-flop is dependent not only upon the positive duration of the clock signal, but also upon the trigger switching time, in conjunction with the total swing of the trigger transition.

Fig. 68 shows the minimum requirement for a trigger pulse, i.e., the relationship between the clock pulse duration, its amplitude, and its fall time for proper triggering. The three graphs shown are all for square wave operation.

Results of the experiments to determine the actual drive capability at specified maximum operating frequencies are shown in Table 9. The drive capability in the JPL specification was exceeded by factors of two or more.

d. Description of tests on gate. To determine the average propagation time for the gate, or decision element, the self-oscillating loop of elements consisted of an odd number of elements 3, 5, 7, 9, or 11. The frequency for 3 units resembled a sine wave of approximately 12 Mc. For higher numbers of elements the waveform was increasingly more square. A flip-flop could be triggered at any point of the loop beginning with five gates in series. The resultant average propagation time was measured at 25–30 nsec.

The same type of tests used with the flip-flop, for determining the maximum operating frequency at specified loads and maximum drive capability at specified frequency, were performed for the decision element. The maximum frequency is defined as the frequency just prior to flip-flop triggering failure. The specified loading rules for maximum loading are:

Five decision element input loads, or

Ten F-F enable loads, or

Two F-F trigger loads.

Included in these loads is the malfunction detector trigger load, equalling two decision element loads or four F-F enable loads.

Results of the experiments to determine the maximum operating frequency, under specified maximum loads, and results of the experiments to determine the actual drive capability at specified maximum frequency, are

Table 9. Results from experiments to determine the actual drive capability for the memory element operating at specified maximum frequency

Type of load	Decision element	Enable	Trigger
Maximum prescribed operating frequency, Mc	3	3	3
Maximum prescribed load	4	8	2
Measured actual drive capability	27	16[a]	9[b]

[a]Triggers grounded.
[b]Enables grounded.

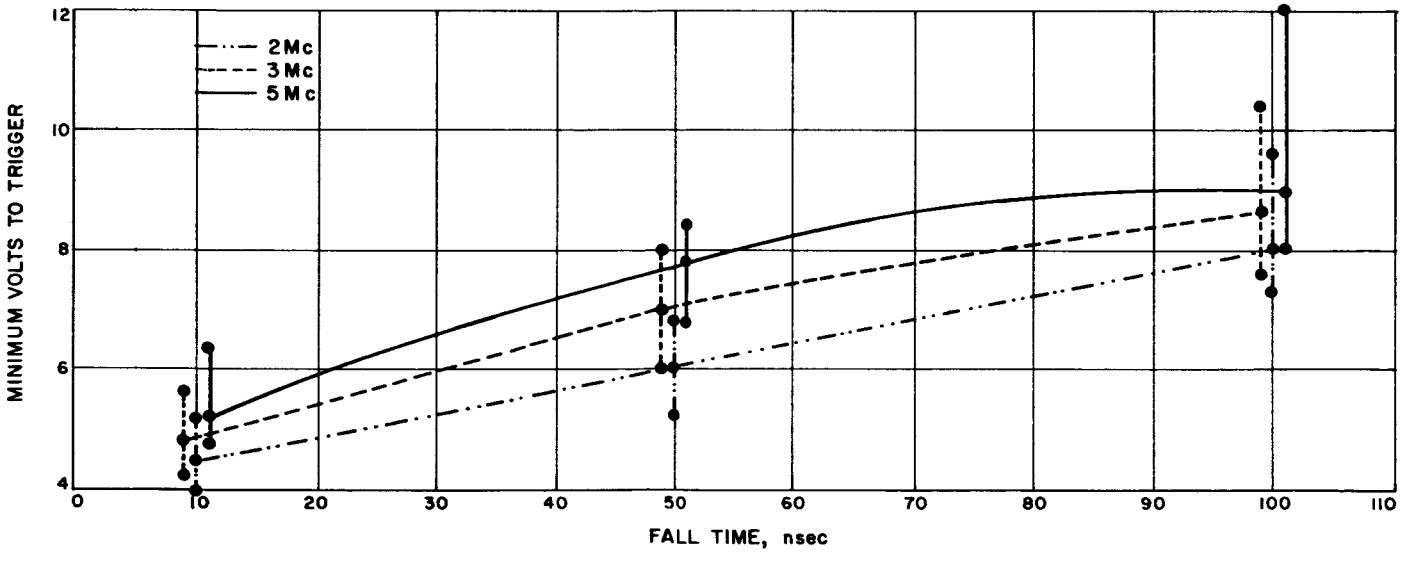


Fig. 68. Amplitude of trigger slope relationship

Table 10. Results from experiments to determine the maximum operating frequency at specified full load for the decision element

Type of load	Decision element	Enable	Trigger
Maximum specified loads	5	10	2
Maximum specified frequency, Mc	3	3	3
Measured operating maximum frequency, Mc	6	6	6

Table 11. Results from experiments to determine the actual drive capability at specified maximum frequency for the decision element

Type of load	Decision element	Enable	Trigger
Maximum specified operating frequency, Mc	3	3	3
Maximum specified load	5	10	2
Measured actual drive capability	12 minimum 37 maximum	30[a]	4 minimum[b] 11 maximum[b]

[a]Triggers grounded.
[b]Enables grounded.

shown in Tables 10 and 11. The operating frequency attained according to this definition is twice the specified frequency of 3 Mc.

Besides these basic tests, the operation of dual level logic, i.e., logic with paralleled collectors, was a matter of special interest. The questions here were: how many units can be paralleled with full load, and how does the output waveform vary with the number of paralleled units? The frequency was held constant at 3 Mc and the full load included the trigger load for the malfunction detector. All other inputs but one, namely, the receiving signal, were grounded. The maximum number of elements that should be paralleled in this manner is 12. The relationship between the number of units in parallel and the output waveform is shown in Fig. 69. The waveform is quite good even for 20 elements paralleled.

e. Test jig. The search for a nonambiguous determination of the system speed of operation for a set of digital circuit modules led to the design of the test jig shown in Fig. 70, a typical systems application of a memory element toggling action. Part of the connection is a number of decision elements.

The clock rate is defined by the memory element *turn-off* delay, plus the propagation time through two

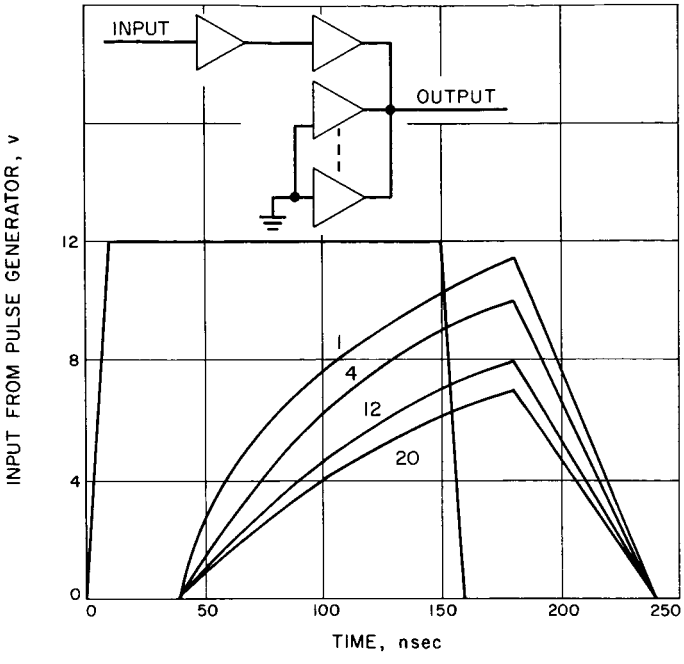


Fig. 69. Output waveforms as a function of the number of gates in parallel

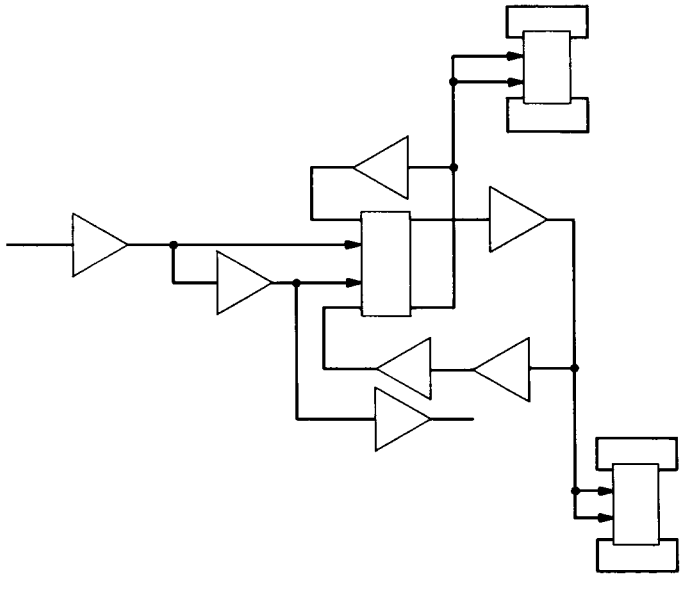


Fig. 70. Logic diagram of quality control test jig

decision elements, plus the required enable prime time that can be fitted into half a clock period. The clock is a symmetrical square wave. Both the set and reset trigger transitions are derived from outputs of decision elements with identical loads. The delay introduced by generating the proper phase of the mid-phase transition is accounted for by two less decision elements in the set-enable branch.

It should be especially noted that with the input clock being symmetrical, the set- and reset-enable times are identical.

Not only did the test jig represent a stringent systems application, but the following worst-case conditions were also enforced:

(1) Temperature: +105°C.

(2) Supply voltages, worst-case combination:

$+24\,v - 10\% = +21.6\,v$,

$+12\,v + 10\% = +13.2\,v$,

$-12\,v - 10\% = -13.2\,v$.

(3) Full asymmetrical load (a combination capacitive trigger load and gate load).

(4) Operating frequency: 2 Mc (4 Mc transition frequency).

(5) One of the gates in the three-gate feedback loop fully loaded.

f. Conclusions. The result is that all modules received to date have successfully passed the quality control test jig described here, operating under these simultaneous worst-case conditions. The modules so far procured under the JPL-owned design have met specifications, and are considered satisfactory as a first iteration on an ultimate uniform basic set of modules of JPL-owned design for use within the entire deep space network (DSN). A further test of these modules will be their use in three advanced engineering systems described elsewhere in this volume: the random pulse generator, the quantile system, and the punctured cyclic coder decoder. A competitive procurement has been initiated for modules for these three systems with the qualified suppliers already mentioned. Also under way is a stringent thermal test of the modules to determine what type of cooling is needed for systems mounted in cabinets. After these tests of the concept of this type of module, the final iteration of choosing a basic set (logic amplifier and diode cluster in addition to flip-flop and gate) can begin. Once the design of the basic set is frozen the peripheral circuits, including delay lines, relay drives and the like, as described in Ref. 44, will be designed and cards will then be produced under these JPL-owned designs. The ultimate goal is a complete set of JPL-owned designs for use in the DSN, with at least five qualified vendors for the entire basic set of four, and at least three for each of the peripheral circuits.

References

1. "Ground Antennas," *SPS 37-20*, Vol. III, pp. 28–34, Jet Propulsion Laboratory, Pasadena, California, March 31, 1963.

2. "Ground Antennas," *SPS 37-26*, Vol. III, pp. 23–29, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

3. "Boresight and Gain Calibrations for DSIF Antennas," *SPS 37-23*, Vol. III, pp. 28–29, Jet Propulsion Laboratory, Pasadena, California, September 30, 1963.

4. "Boresight and Gain Calibrations for DSIF Antennas," *SPS 37-24*, Vol. III, pp. 30–33, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

5. "Boresight Calibrations for DSIF Antennas," *SPS 37-25*, Vol. III, pp. 21–25, Jet Propulsion Laboratory, Pasadena, California, January 31, 1963.

6. "Feeds and Feed Systems," SPS 37-18, Vol. III, pp. 24–27, Jet Propulsion Laboratory, Pasadena, California, November 30, 1962.

References (Cont'd)

7. "Prototype S-Band Monopulse Cassegrain System," *SPS 37-18*, Vol. III, pp. 65–68, Jet Propulsion Laboratory, Pasadena, California, November 30, 1962.

8. "Radio Calibration Techniques," *SPS 37-26*, Vol. III, pp. 26–27, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

9. "Temperature Calibrations of Microwave Terminations," *SPS 37-25*, Vol. IV, pp. 118–121, Jet Propulsion Laboratory, Pasadena, California, February 29, 1964.

10. "S-Band Rotary Vane Attenuator," *SPS 37-24*, Vol. IV, pp. 156–161, Jet Propulsion Laboratory, Pasadena, California, December 31, 1963.

11. "S-Band Rotary Vane Attenuator," *SPS 37-25*, Vol. IV, pp. 128–132, Jet Propulsion Laboratory, Pasadena, California, February 29, 1964.

12. "S-Band Antenna Gain and Pattern Calibrations," *SPS 37-24*, Vol. III, pp. 24–27, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

13. Seidel, B., "Simultaneous Lobing Radiometric Tracking System," *SPS 37-26*, Vol. IV, pp. 216–220, Jet Propulsion Laboratory, Pasadena, California, April 30, 1964.

14. Manasse, R., "Maximum Angular Accuracy of Tracking a Radio Star by Lobe Comparison," *IRE Transactions on Antennas and Propagation (Professional Group)*, pp. 50–56, January 1960.

15. Mehuron, W. O., "Passive Radar Measurements at C-Band Using the Sun as a Noise Source," *The Microwave Journal*, pp. 87–94, April 1962.

16. Kennedy, J. T., and Rosson, J. W., "The Use of Solar Radio Emission for the Measurement of Radar Angle Errors," *Bell System Technical Journal*, pp. 1799–1812, November 1962.

17. "Scale Model Feed for AAS," *SPS 37-26*, Vol. III, pp. 72–75, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

18. "100-kw S-Band Transmitter," *SPS 37-26*, Vol. III, pp. 30–31, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

19. "100-kw S-Band Transmitter," *SPS 37-24*, Vol. III, p. 46, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

20. "High-Power 100-kw S-Band Transmitter," *SPS 37-25*, Vol. III, p. 32, Jet Propulsion Laboratory, Pasadena, California, January 31, 1964.

21. "Mod III Ranging Equipment," *SPS 37-21*, Vol. III, pp. 62–73, Jet Propulsion Laboratory, Pasadena, California, May 31, 1963.

22. "Ranging Coders," *RS 36-6*, p. 43, Jet Propulsion Laboratory, Pasadena, California, December 1960.

23. "30-ft Diameter Azimuth-Elevation Antenna," *SPS 37-19*, Vol. III, pp. 32–35, Jet Propulsion Laboratory, Pasadena, California, January 31, 1963.

24. "30-ft Diameter Azimuth-Elevation Antenna," *SPS 37-20*, Vol. III, pp. 28–31, Jet Propulsion Laboratory, Pasadena, California, March 31, 1963.

25. "2.388 Gc Receiver," *SPS 37-17*, Vol. III, pp. 32–33, Jet Propulsion Laboratory, Pasadena, California, October 1, 1962.

26. "Mod III Transmitting System, 2388 Mc, 100 kw," *SPS 37-22*, Vol. III, p. 17, Jet Propulsion Laboratory, Pasadena, California, July 31, 1963.

References (Cont'd)

27. "Mod III Transmitting System, 2388 Mc, 100 kw," *SPS 37-24*, Vol. III, pp. 51–53, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

28. "Monostatic Satellite and Lunar Radar Receiver Module Development," *SPS 37-26*, Vol. III, pp. 45–46, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

29. "Central Frequency Synthesizer," *SPS 37-25*, Vol. III, pp. 37–38, Jet Propulsion Laboratory, Pasadena, California, January 31, 1964.

30. "Mod IV Planetary Radar Receiver, 2.388 Gc," *SPS 37-21*, Vol. III, pp. 49–61, Jet Propulsion Laboratory, Pasadena, California, May 31, 1963.

31. "RF Voltage Controlled Oscillator Developments," *SPS 37-15*, Vol. III, pp. 34–36, Jet Propulsion Laboratory, Pasadena, California, May 31, 1962.

32. Solomon, G., and Stiffler, J., "Punctured Systematic Cyclic Encoder-Decoder," *SPS 37-23*, Vol. IV, pp. 149–151, Jet Propulsion Laboratory, Pasadena, California, October 31, 1963.

33. Posner, E. C., and Solomon, G., "A Code Over the 32 Element Field for Use on Interstation Teletype Channels," *SPS 37-26*, Vol. IV, pp. 223–225, Jet Propulsion Laboratory, Pasadena, California, April 30, 1964.

34. Easterling, M., Eisenberger, I., and Posner, E. C., "Data Compression by Quantiles," *SPS 37-17*, Vol. IV, pp. 74–78, Jet Propulsion Laboratory, Pasadena, California, October 31, 1962.

35. Eisenberger, I., and Posner, E. C., "Systematic Statistics Used for Data Compression in Space Telemetry," Technical Report No. 32-510, Jet Propulsion Laboratory, Pasadena, California, October 1, 1963.

36. "Development of Digital Circuit Modules," *SPS 37-24*, Vol. III, pp. 83–97, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

37. Viterbi, A. J., "On Coded Phase-Coherent Communications," Technical Report No. 32-25, Jet Propulsion Laboratory, Pasadena, California, August 15, 1960.

38. Golomb, S. W., "Sequences with Randomness Properties," Glenn L. Martin Co., Baltimore, June 1955.

39. Peterson, W. W., "Error-Correcting Codes," John Wiley & Sons, Inc., New York, N. Y., 1961.

40. "Development of Digital Circuit Modules," *SPS 37-24*, Vol. III, pp. 83–95, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

41. Zierler, N., "Linear Recurring Sequences," *Journal of the Society for Industrial and Applied Mathematics*, Vol. 7, No. 1, pp. 31–48, 1959.

42. Feller, W., "An Introduction to Probability Theory and Its Applications," Second Edition, John Wiley & Sons, Inc., New York, N. Y., 1957.

43. Eisenberger, I., "Genesis of Bimodal Distributions," *SPS 37-18*, Vol. IV, pp. 178–180, Jet Propulsion Laboratory, Pasadena, California, December 31, 1962.

44. "Development of Digital Circuits Modules," *SPS 37-24*, Vol. III, pp. 83–95, Jet Propulsion Laboratory, Pasadena, California, November 30, 1963.

VII. Advanced Antenna System

A. Summary

A 210-ft-diameter Advanced Antenna System (AAS) is being designed and constructed for the Mars Station at Goldstone. This AAS is designed specifically for deep space communications and will be integrated with related systems and equipment at the Goldstone Station of the Deep Space Instrumentation Facility (DSIF). The antenna will operate initially at the S-band frequencies of 2.1 to 2.3 Gc. Work on the AAS project has been reported regularly in *SPS*, and since the last reporting period the erection of the pedestal and the final design of the basic antenna (by Rohr Corp.) have been nearly completed. Work has begun, under subcontract, for the integrated power system for the AAS. Preliminary design and specification work has been done on the precision data system, including the master equatorial instrument.

B. Contractor-Furnished System

The Rohr Corp. is presently completing the final design phase for the antenna structure and drive system and is starting the procurement and fabrication phases. A cross sectional drawing and brief description of the major components of the AAS were included in Ref. 1.

The major concrete work for the antenna pedestal–foundation will soon be completed. Backfill and compaction inside and outside of the pedestal was accomplished in March 1964 and all material was compacted, exceeding specification. The placement of concrete (273 yd^3) for the instrument tower was also completed in March. The pedestal walls are finished and preparations are being made for the placement of concrete for the top deck of the pedestal (Fig. 1). Aquapon paint is being applied

to the outside concrete surfaces to reduce shrinkage rate by retarding hydration.

The underground installation for water and electricity has been completed and construction work is in progress for installation of these services within the pedestal. The concrete first floor slab has been placed (Fig. 2), along with the structural beams for the second floor. Fig. 3 is a side view of the outside of the pedestal showing construction progress as of April 9, 1964.

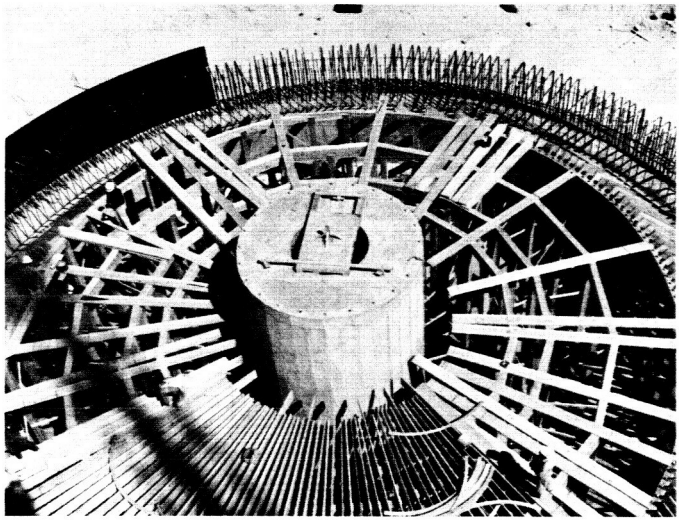


Fig. 1. Forming the pedestal top deck

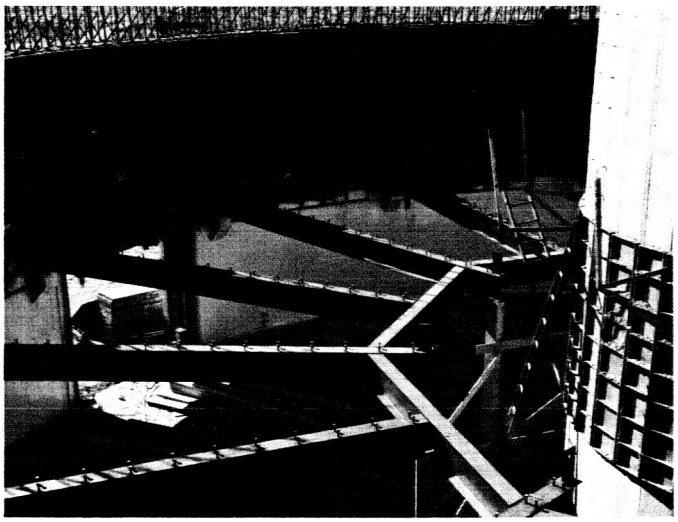


Fig. 2. Placement of structural beams for the pedestal second floor

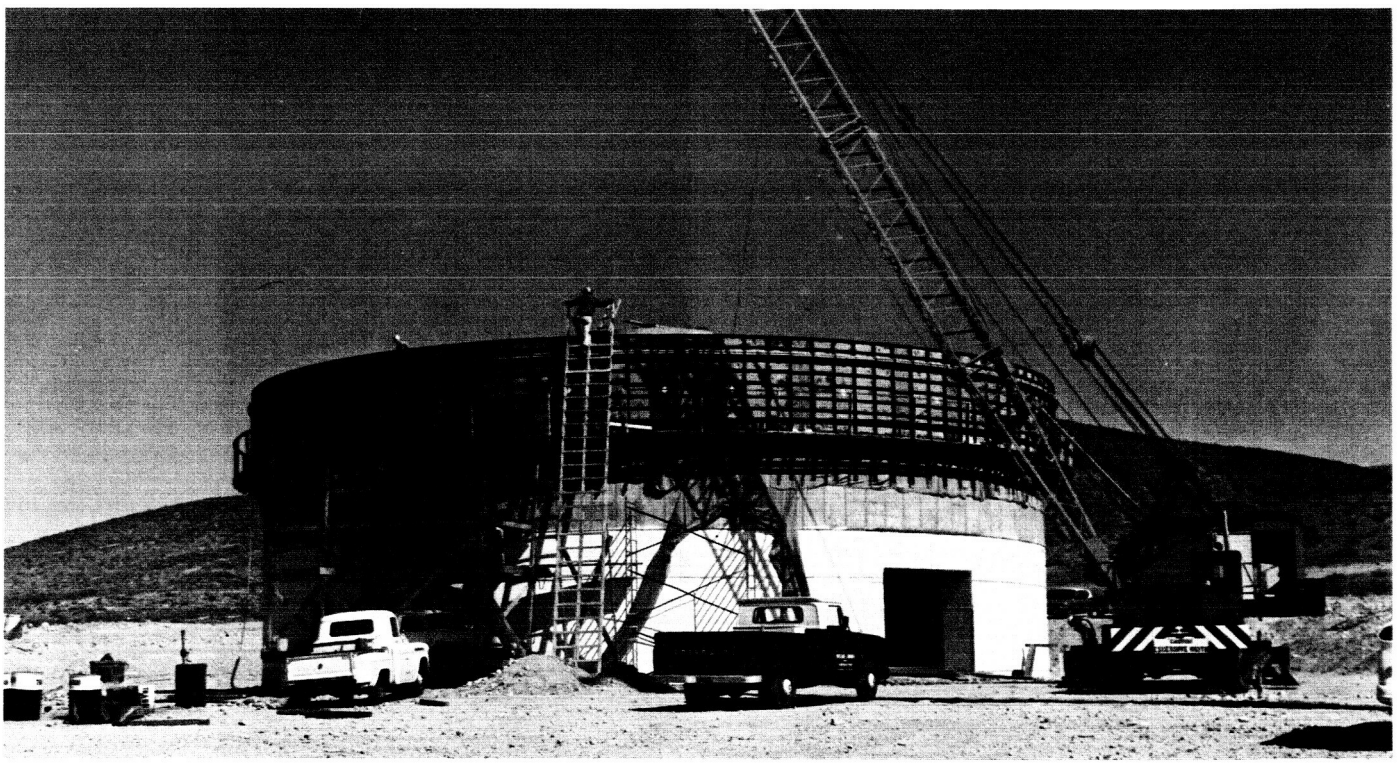


Fig. 3. Pedestal construction as of April 9, 1964

Concrete (505 yd^3) was placed for the pedestal haunch on April 16, 1964. Figs. 4 and 5 depict the concrete placement and site construction. The pedestal haunch will carry the runner for the hydrostatic thrust bearing and, therefore, the placement of reinforced concrete was highly critical. Each load of concrete was carefully tested and the placement closely supervised. Shrinkage measurements will be made at regular intervals on the pedestal.

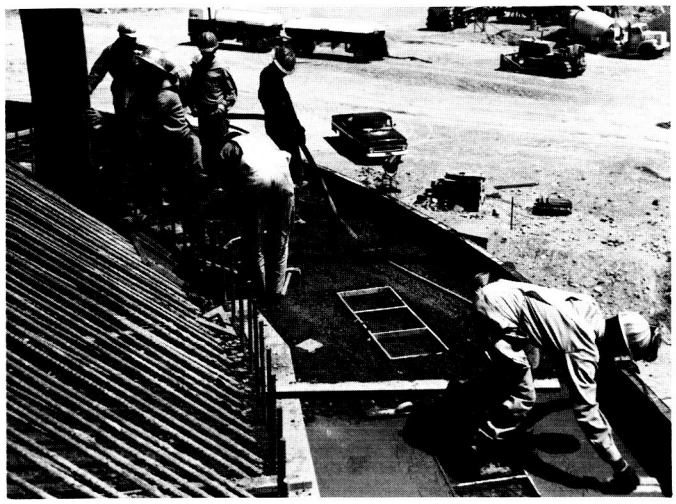


Fig. 4. Concrete placement for the pedestal haunch

The final detail design of the antenna structure above the pedestal continues at Rohr Corp. System integration studies are being up-dated as final design progresses. The subreflector final design has been completed and a final computer run for the dynamic analysis of the quadripod (lateral and transverse modes) is in process. Final design of the feed cone handling system is nearing completion. The method for mounting the primary reflector panels to the backup structure has been resolved; a ball joint socket-type adjustment mechanism will be used. The primary reflector structure deflections are being checked at JPL by computer analysis. Certain structural members are being resized and final JPL check analysis is being made. Work is continuing on the final dynamic runs of the elevation wheel and its connections and member areas. Alidade and elevation bearing assembly final design drawings have been completed. Material orders have been placed and fabrication will begin soon. The

Fig. 5. Aerial photograph of on-site progress as of April 16, 1964

design of the elevation bearing tie truss is nearing completion. Final design of the elevation and azimuth drives continues and initial fabrication of the gear blanks is under way. Progress has been steady in all design areas of the servo drive and control system. Final design and detailed drawings of the hydrostatic thrust and radial bearing have progressed sufficiently to enable placement of material orders. Fabrication of portions of this component area has begun.

C. Site Development

Site development is continuing. A contract was awarded in March 1964 for the diesel electric power installation. Three 2400-v, 1200-rpm, 500-kw diesel powered electric generators with associated switch gear, fuel oil tankage, concrete block building and associated facility services will be provided. This equipment will be used for late construction phase power for the AAS and also as the primary power source for the Mars Station during mission operations.

D. Precision Angle Data System

The AAS will use a precision angle data system (Fig. 6) to determine the angular position of the antenna beam. To overcome the structural deflection and alignment problems associated with on-axis encoders, optical links are used to measure the angular orientation of the center core of the reflector structure with respect to a ground referenced instrument, the master equatorial (ME). Preliminary design analysis of the ME was presented in Ref. 2. The angular orientation of the reflector structure is represented by the intermediate reference structure (IRS).

There will be two basic modes of precision operation for the AAS, RF autotrack and pointing. In the RF autotrack mode, the antenna is servoed to follow the RF signal from the spacecraft. To provide precision readout of the beam position in the RF autotrack mode, the ME is slaved by means of the optical link and the IRS to the reflector orientation. In pointing modes, the process is reversed; the ME is commanded in hour angle–declination (HA–Dec) coordinates and the antenna is slaved to it.

The subsystems of the AAS precision angle data system are:

a. Optical instrument mount. The design of the optical instrument mount will be based on conventional optical telescope practice. Fig. 7 is a preliminary sketch showing the mount and its relationship to the rest of the system. As shown in the figure, a fork configuration will be used, with the optical link equipment mounted on the declination axis. The axes of the mount have a 2-in.-diameter clear bore so that precision optical tooling can be used to align the mount.

b. Servo drives and controls. A linear servo system using dc torquers will be used to control the ME. The position error signals to command the servo are derived from the optical subsystem and from analog or digital data subsystems.

In addition to the servo drive, a sidereal rate drive is provided for use as a backup and for testing in pointing mode operation. It is an open loop system, the accuracy of which depends on the accuracy of the gearing and the stability of the frequency source. Controls are provided to add small differential rates to the basic sidereal rate.

c. Optical link subsystems. This subsystem includes the mirrors and the two axis automatic autocollimators which are required for slaving the antenna to the ME or the reverse. In pointing modes, an autocollimator mounted on the IRS develops tracking error signals in El and cross El coordinates for the antenna servos by reflecting a collimated beam of light off a mirror located on the ME and comparing the reflected beam to the original beam. In the autotrack mode, an autocollimator located on the ME and a mirror on the IRS are used, and the resulting HA–Dec coordinate error signals control the ME servos.

d. Special structural elements. The special structural elements are:

(1) *Intermediate reference structure.* The intermediate reference structure (IRS) is located behind the primary reflector; its purpose is to accurately represent the angular orientation of the RF beam. Compensation of IRS to correct for structural dead load errors will be used to improve system accuracy. The autocollimators and mirrors

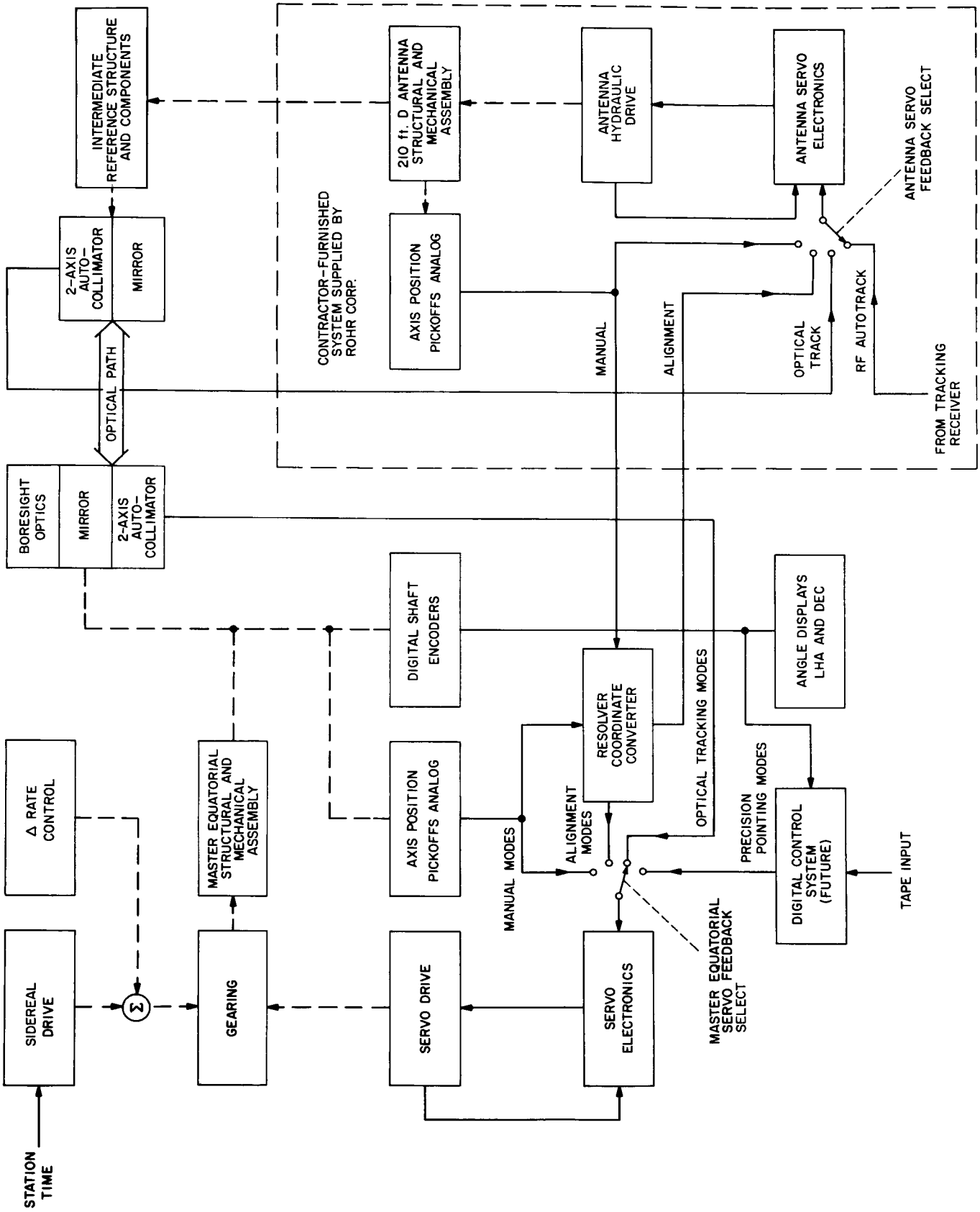


Fig. 6. AAS precision angle data system simplified block diagram

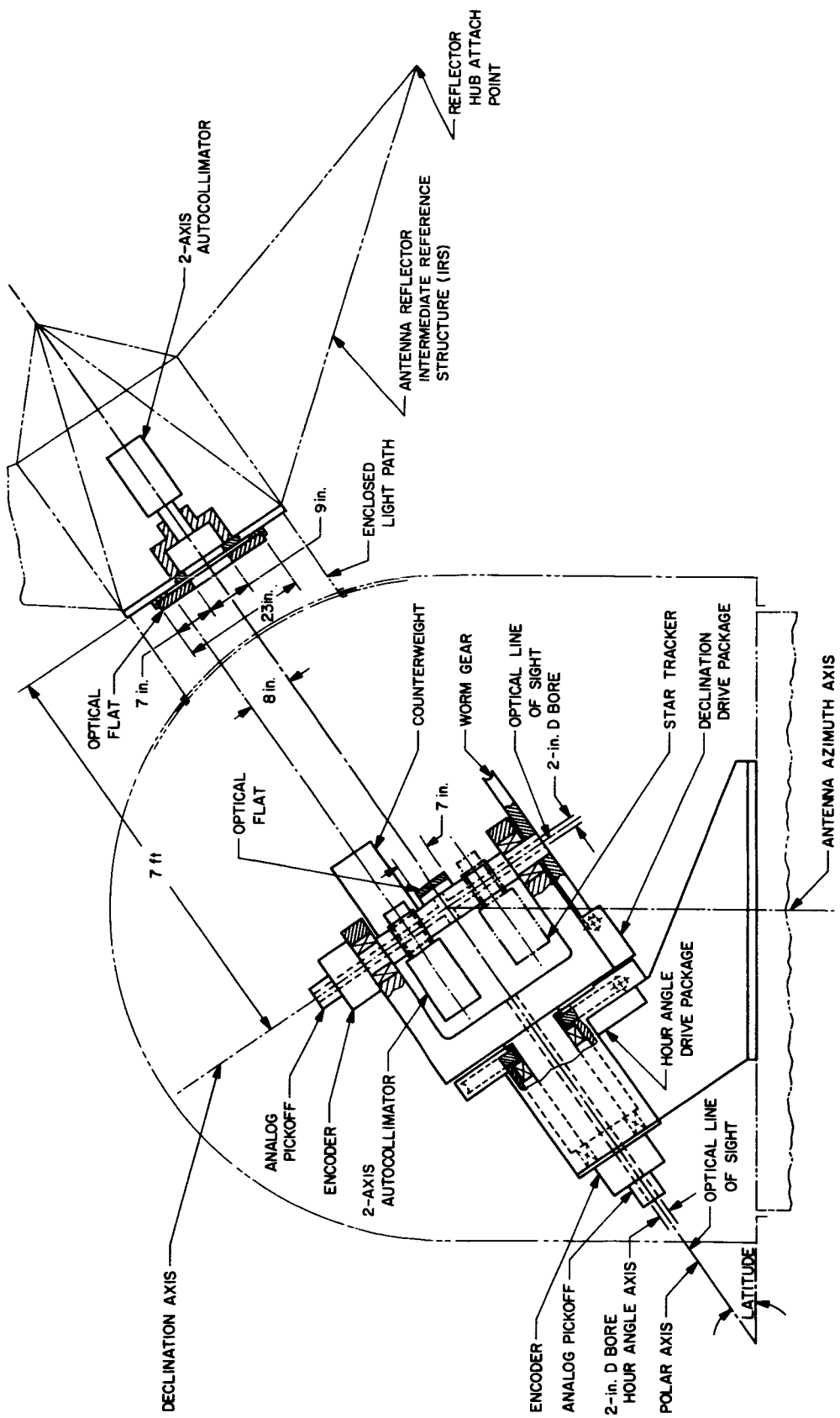


Fig. 7. Sketch of precision angle data system

of the antenna end of the optical link are mounted on the IRS.

(2) *Instrument tower.* The ME will be supported at the intersection of the antenna axes by an isolated wind and thermal shielded instrument tower designed so that its natural frequency will be greater than 5 cps with the instrument mount installed on top.

(3) *Astrodome and enclosed light path.* The ME must be isolated from the external environment. To do this, an astrodome protective housing will be mounted on top of the thermal shield so that it rotates with the azimuth axis of the antenna. The front face of the astrodome is cylindrical and a tube extends from this face to the IRS. The tube rotates with the elevation axis of the antenna and encloses the light path between the autocollimators and the mirror surface.

(4) *Air conditioning equipment.* Air conditioning equipment will be provided to control the environment in the astrodome, the IRS, the enclosed light path, and the area between the thermal shield and the instrument tower. The temperature in these areas will be maintained at 72 $\pm 2°$F.

e. Resolver coordinate converter. A low-accuracy resolver coordinate converter (RCC) will be provided to convert the Az–El coordinates of the antenna to the HA–Dec coordinates of the ME so that the ME can be aligned to the antenna within the capture angle of the autocollimators. The unit will also be reversible so that the antenna can be aligned to the ME. In addition to the alignment function, the coordinate converter will be used for secondary commands to the antenna in HA–Dec coordinates.

f. ME boresight optics. An optical package will be mounted on the Dec axis for checking the final alignment of the ME by means of optical star tracks. The unit may be combined with the autocollimators to reduce the size of the equipment mounted on the Dec axis.

g. Digital angle encoders. Digital shaft angle encoders will be directly coupled to both the HA and the Dec shafts of the ME. The resolution of these encoders will be 1 part in 2^{20} and the error will be less than 5 sec of arc peak. Outputs are provided in binary-coded decimal for recording and display and in binary code for use with a future digital control system. Light bank displays are provided as part of the present system.

The digital control system will allow the antenna to be controlled from punched paper tape or to be slaved to the Echo Station computer for two-station operation. Plans for providing this system are not yet definite.

References

1. "Synopsis," *SPS 37-26*, Vol. III, pp. 66–72, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

2. "Master Equatorial Preliminary Design Analysis," *SPS 37-26*, Vol. III, pp. 73–79, Jet Propulsion Laboratory, Pasadena, California, March 31, 1964.

Errata

The following corrections should be noted for *SPS 37-26*, Vol. III:

1. Cover and title page: "January 1, 1963" should read "January 1, 1964."
2. Page 7: Transpose Figs. 2 and 3, photographs only.
3. Page 31: Fig. 8 should appear as

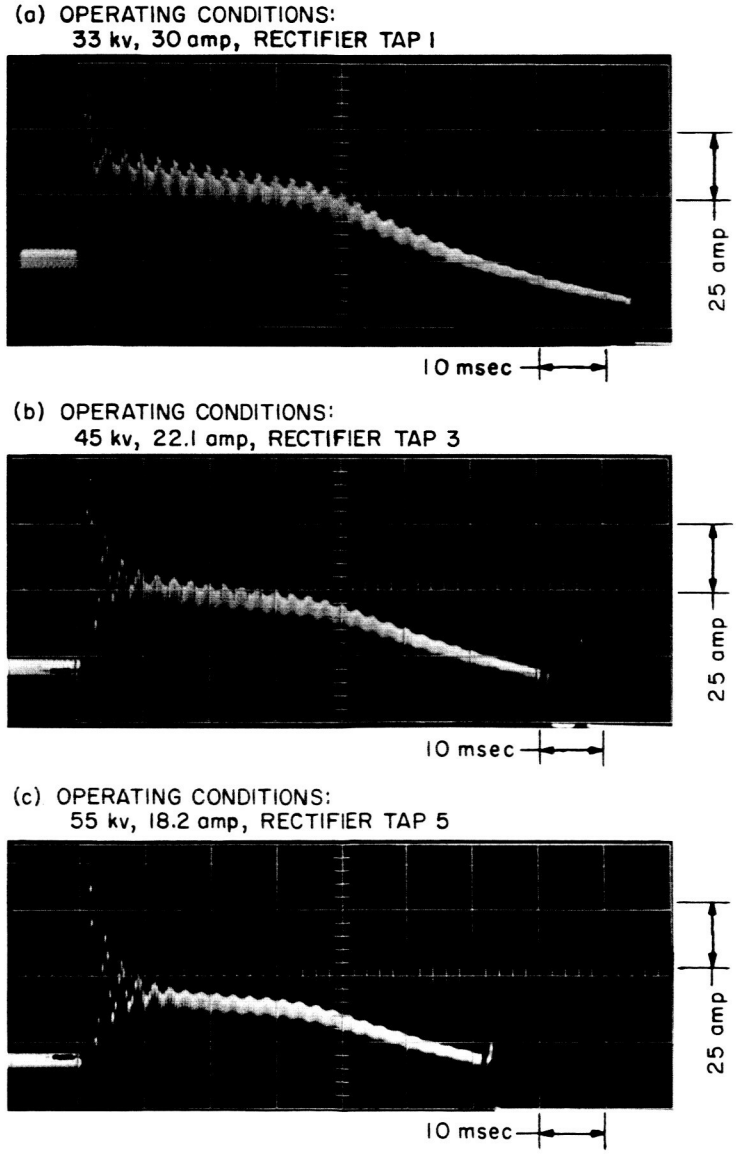


Fig. 8. Current discharge waveforms seen by the rectifier tubes during crowbar operation

4. Page 31 and 32: Transpose Figs. 9 and 10, photographs only.
5. Page 32: "(See part *d* of this article.)" should read "(See part *d* of *10-kw S-Band Transmitter*, pp. 47 and 48.)."